How to Use the LX7730 Evaluation Board

Table of Contents

Introduction

The LX7730 is a spacecraft telemetry manager IC that contains a 64 universal input multiplexer that can be configured as a mix of differential or single ended sensor inputs. There is also a programmable current source that can be directed to any of the 64 universal inputs. The universal inputs can be sampled with a 12 bit analog-to-digital converter at a sample rate up to 13 kHz. The universal inputs can also function as variable bi-level inputs with the threshold set by an internal 8 bit digital-to-analog converter. There is an additional 10 bit digital-to- analog current DAC with complementary outputs. Finally there are 8 fixed threshold bi-level inputs.

The LX7730 is register programmable with 17 addressable eight bit registers. Two options are available for communication with the host FPGA. First there is an eight bit parallel bus with 5 address bits and a read/write bit that can communicate at a speed of up to 25MHz. The second option is a pair of 12.5Mbps SPI interfaces that can support redundant (alternating not simultaneous) communication to two different hosts.

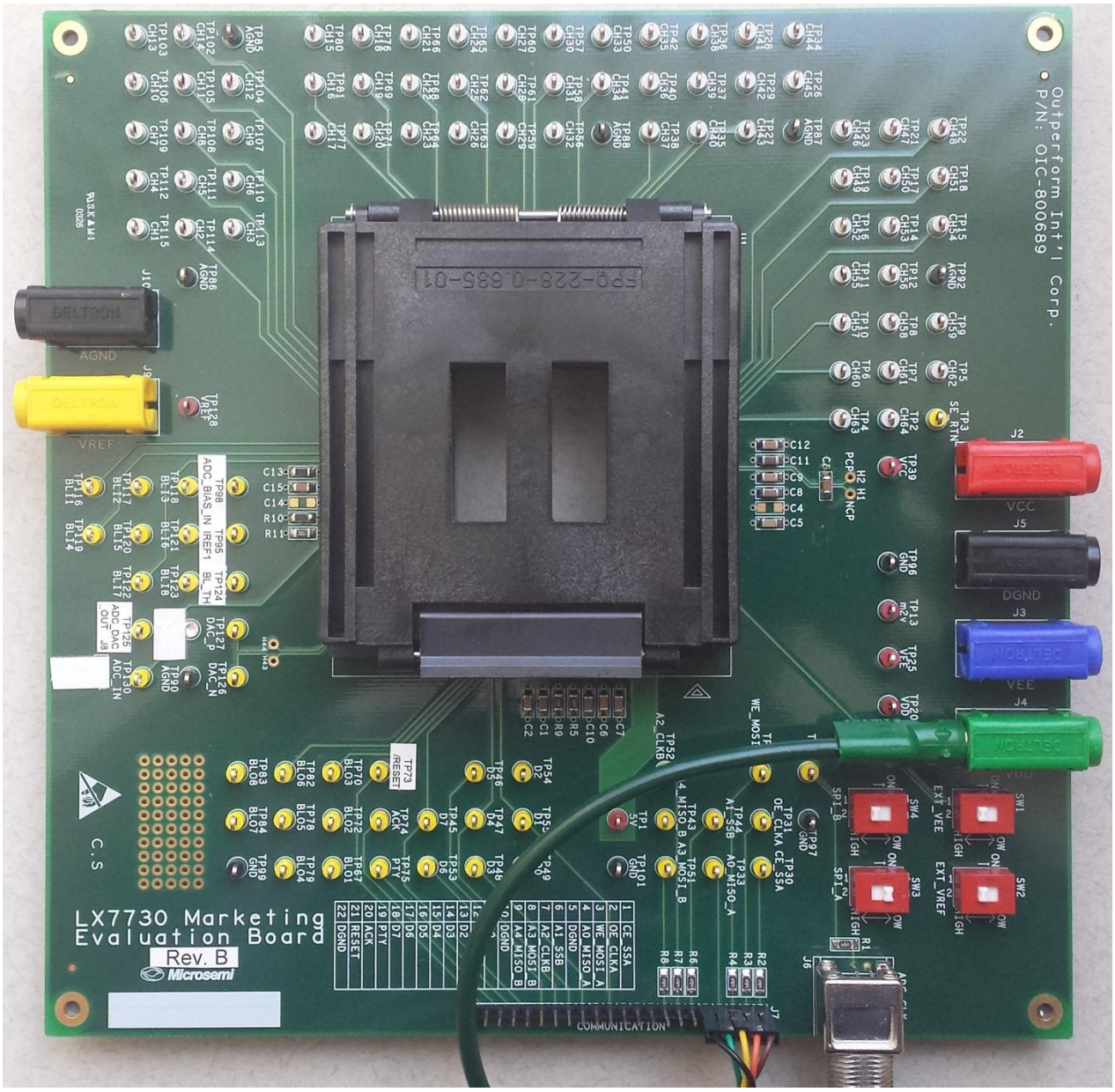
The LX7730 Evaluation board is basically a ‘breakout box’ that allows the user when it’s coupled with the included USB to serial interface and application software to exercise the controller’s features. The included USB to serial interface is the Future Technologies Device International (FTDI) C232HM-DDHSL-0 cable assembly. USB device drivers must be loaded on host computer along with the LX7730 application software to utilize the LX7730 evaluation board as shipped.

Kit Contents – LX7730-EVB

LX7730 Evaluation Board

FTDI C232HM-DDHSL-0 USB to MPSSE cable w/ 3.3V logic Signals

Windows Device Drivers and LX7730 Software GUI, LX7730 User Guide & LX7730 Evaluation Board Schematic



LX7730 Evaluation Board

Setup Procedure

SOFTWARE

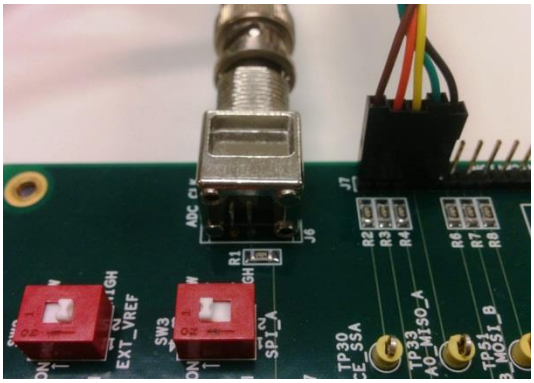
Copy the FTDI C232HM-DDHSL-0 USB MPSSE cable device drivers (CDM v2.10.00 WHQL Certified.zip) and LX7730 software GUI (LX7730.zip) to a directory on your local PC from the thumb drive.

Install the FTDI device drivers on your local PC, once installed when you plug in the C232HM-DDHSL-0 cable your device manager (under Ports (COM & LPT) should indicate a USB Serial Port device is active. You can check this by going to Windows Control Panel, Device Manager, Ports, and select the USB port with the adapter. It should say device is working properly. Additional details about the FTDI cable can be found in their datasheet included (DS_C232HM_MPSSE_CABLE.pdf).

HARDWARE CONNECTIONS

You must connect the DS_C232 cable to the board as follows (if using the LX7730 Software GUI) to SPI bus A and the 3.3V supply built into the cable to power VDD supply of the LX7730:

J7- LX7730 Eval Board	C232HM-DDHSL-0
Pin 1 – ce_ssa	Pin 5- CS - Brown
Pin 2 – ce_clka	Pin 2 – SK - Orange
Pin 3 – we_mosi_a	Pin 3 – DO - Yellow
Pin 4 – a0_miso_a	Pin 4 – DI - Green
Pin 5 - DGND	Pin 10 – GND - Black
J4 – VDD	Pin 1 – 3.3V - Red



SW3 on the evaluation board should also be in the ON position enabling the IC to utilize the SPI_A serial input, or you can use SPI_B and pins 6 to 10 and move SW4 to ON position instead.

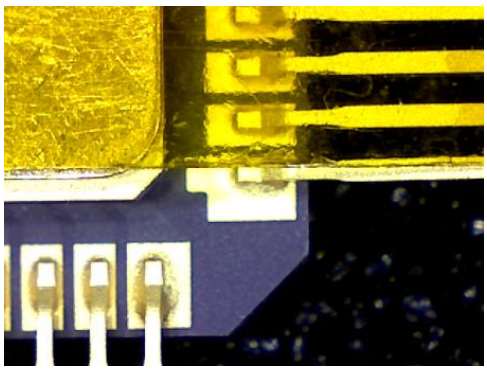
As noted in the last row of the table above the serial cable is capable of supplying the 3.3V VDD logic supply.

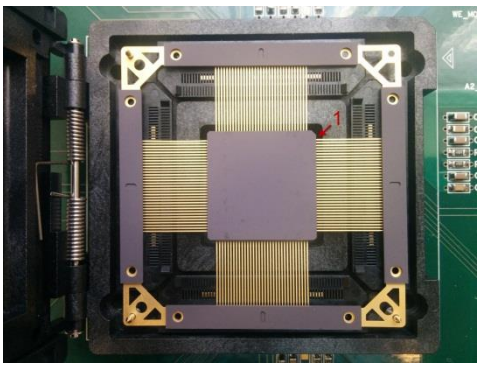
Use an external power supply to provide 12V to 16V (nominally 15V) to VCC. Set power supply's current limit to a minimum of 300mA if slewing the supply slowly and utilizing the controller's internal charge pump to generate VEE. Also connect a frequency generator to supply a 500 kHz 3.3V square wave signal on the CLK input (BNC).

Before putting the LX7730 in the socket turn-on the power supply and verify that all the voltages (VCC and VDD are correct and the clock signal is enabled. Turn off the power supplies.

PLACING THE IC IN THE SOCKET

With the socket open pin one 1 of the socket is the corner that does not have a metal guide pin and is in the upper left corner nearest the four power banana jacks. The IC is placed ceramic side up. Identify the pin 1 one indicator finding the small additional metal tab on the lead as shown in the photo below left.





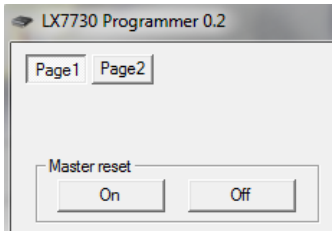
Powering on the Device

Execute the GUI software (LX7730.exe). Then, apply VCC to the evaluation board. (AGND and VREF do not require connections). At this point you can use a DMM to measure and validate voltages at VEE (TP25), m2v (TP13), VREF (TP128) and 5V (TP1). Check that there is communication by reading the Function Enable register which should put checks in each box. Also verify that the 500 kHz and 3.3Vpp square wave (from an external function generator) is applied to the BNC connector (or the ADC won't function).

To execute a command in the GUI, you must enter the information for the section and then push the soft Write button for the section; you can then select the Read button for the section to verify the command was received. (Entering information without a Write will do nothing.)

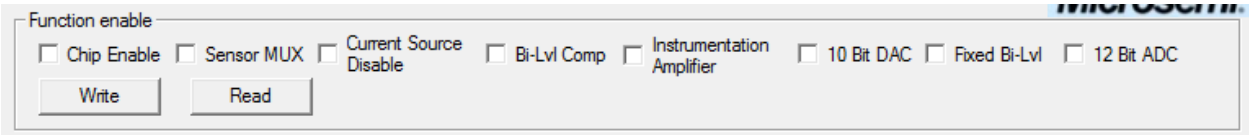
Using the Software GUI

MASTER RESET



Master reset button is used to perform a master reset which returns all internal registers to the power on (default) state.

FUNCTION ENABLE



The Function enable screen provides the option to power down selected functions that are not needed; the default state is everything enabled as indicated. This feature allows user the flexibility to conserve power while keeping needed functions alive.

After starting the GUI and the evaluation board power supplies, perform a READ and then WRITE process to insure the IC in enabled. IT IS RECOMMENED TO READ BACK AND VERIFY THE ACTUAL STATE OF THE LX7730'S REGISTERS, AND IF NECESSARY WRITE AGAIN.

At this point you can verify that the various LX7730 internal supplies are up and working.

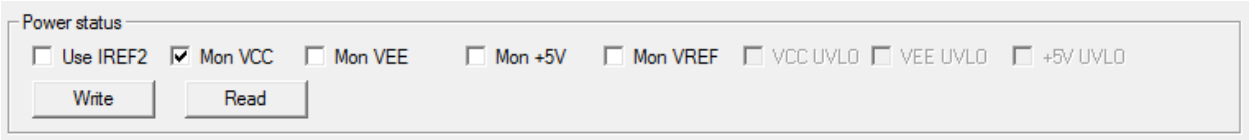
Name	Test Point	Measured Voltage
VCC	TP39	Externally supplied voltage, nominally 15V
M2v	TP13	-2V
VEE	TP25	About -10V if using the internal charge pump to generate VEE
VDD	TP20	+3.3V (supplied by the USB cable)
CLK	TP24	Used to verify your external 3.3V square wave input
5V	TP1	+5V
VREF	TP128	+5V (this voltage is adjustable and or can be disabled and an external reference voltage applied)

The default condition and description Function Enable Register is shown below:

Function Enable Register

Name	Default	Description
Chip Enable	1	If de-asserted everything but the active power supplies and digital interface to the FPGA is turned off but the internal register contents are preserved; this is a low power sleep mode. CH# and BLI# and DAC pins are cold spared. If de-asserted, functions corresponding to bits 0 thru 6 are disabled.
Sensor MUX	1	If de-asserted, all CH switching and routing (Analog or Bi-Level) is turned off. CH# pins are cold spared.
Current Source Disable	1	If asserted, the multiplexed current source directed to a CH# pin is not used and powered down. If de-asserted, the multiplexed current source is enabled and directed to the CH# selected in the Analog MUX section.
Bi-level comp	1	If de-asserted, power is removed from the bi-level comparators but doing so does not affect the functionality of the Analog Multiplexer and ADC.
Analog Amplifiers	1	If de-asserted, the instrumentation amplifier is powered down. The ADC and Bi-level comparators are not affected; however the ADC must be driven by an external signal using ADC_IN pin (with Filter Off bit asserted or ADC=Hi Z asserted).
10 Bit DAC	1	If de-asserted, the 10 bit DAC is not used and powered down. DAC outputs are cold spared.
Fixed Bi-Level	1	If de-asserted, the Fixed Bi-level converters are not used and powered down. BLI# inputs are cold spared.
12 Bit ADC	1	If de-asserted, the 12 bit ADC is not used and powered down.

POWER STATUS



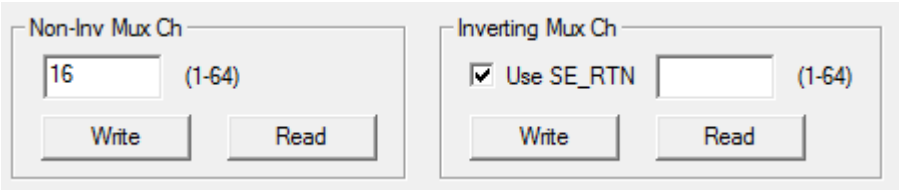
The power supply pins for the LX7730 can be monitored by selecting special calibration registers: MON VCC, MON VEE, MON +5V, MON VREF. The voltages are divided down by a factor of 6 for the VCC & VEE rails and a factor of 2 for the 5V and VREF pins and routes the selected pin voltage to the non-inverting terminal of the IA (instrumentation amplifier). It overrides the setting of the Analog MUX Inverting MUX Channel and applies GND to the inverting terminal of the Instrumentation Amplifier for the positive voltages and GND to the non-inverting input of the IA for Mon VEE.

For example if Mon VCC is selected as shown above and the Signal Conditioning Amp Gain Setting is set to a gain of 0.4 and the ADC Controls Auto Conv box is checked then when reading the ADC a measurement of about 1V should be indicated. (15V divided by a gain of 6 (internal divider), times 0.4 (gain setting)

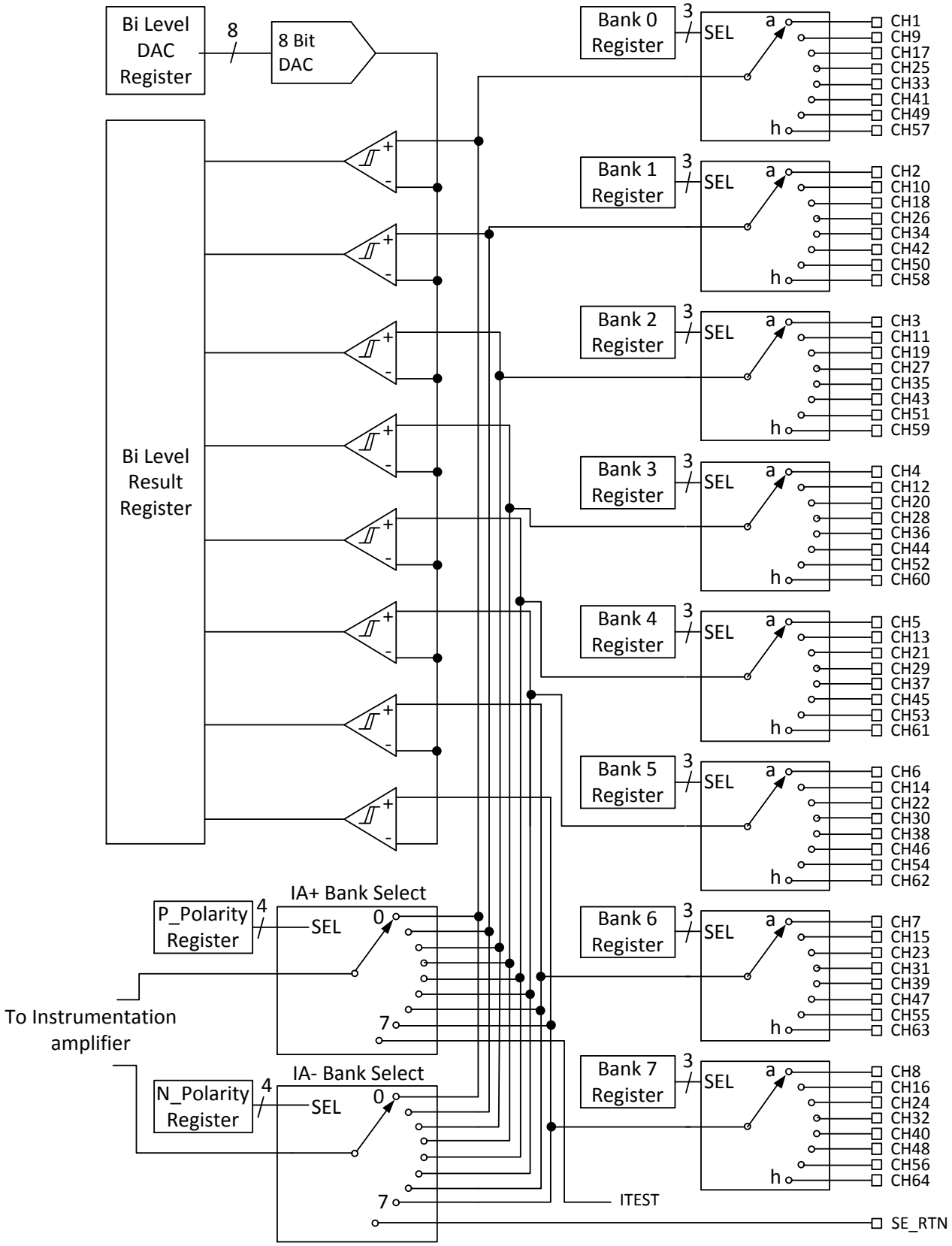
The LX7730 provides a redundant precision reference current IREF2 which can be selected should IREF 1 (TP95) fail. The GUI allows selection of IREF2 internal IC resistor by checking the box in the Power Status window.

The VCC UVLO, VEE UVLO and +5V UVLO flags will be asserted when VCC, VEE, or +5V respectively are below their corresponding UVLO thresholds. To find the UVLO status for any of these supplies select the Read button, and look for the corresponding status box check mark. They are greyed-out since they are output only and cannot be selected.

ANALOG MUX



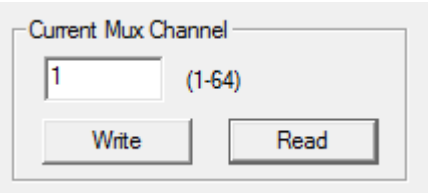
The analog multiplexer (AMUX) consists of 64 inputs. The Bi-level MUX and the AMUX are not independent; the En BL Sw Pos (found in the Bi-level Bank Switch Position section page 9) must be de-selected in order to use the AMUX. For a single ended input measurement the common SE_RTN reference pin can be selected checking the box Use SE_RTN. When selecting SE_RTN then TP3 SE_RTN pin is used as a common return for single ended sensor inputs. When using differential sensor inputs since the AMUX is physically divided into eight banks of eight inputs. Only one CH#, from one input bank can be selected at a time which means that differential measurements must consist of two CH#s from two different input banks. For example CH1 can be connected with any other channel number except those in Bank 0 (i.e. CH9, 17, 25, 33, 41, 49 and 57) See the Sensor Multiplexer Block Diagram that follows:



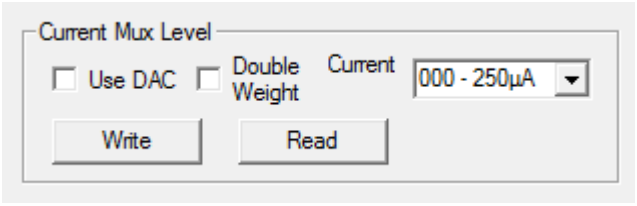
Sensor Multiplexer Block Diagram

CURRENT DE-MUX

The current de-mux routes a programmable current to whichever of the 64 channel inputs is selected. The default channel in CH1, the default current is 250µA. There are several modes of operation depending on the current amplitude required.

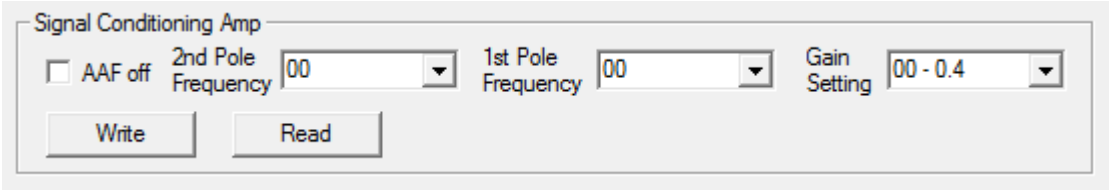


There are eight selectable levels range from 250µA to 2mA using the drop down box. When the Double_Weight box is checked the selected value is doubled for a range from 500µA to 4mA. If the Use DAC box is selected, the 10bit DAC is used to set the de-mux current instead of the programmable current source; each LSB has a weight of 10µA. A maximum of 300µA is suggested (code 31) when operating in this mode. The current de-mux can be shut off selecting the Current Source Disable box in Function Enable; the current De-MUX defaults to the off state at power up and must be selected to activate.



SIGNAL CONDITIONING AMP

The instrumentation amplifier, anti-aliasing filter, and ADC range scaling reside between the output of the analog multiplexer and the input to the ADC. The output of the entire gain and filter stage is accessible at the pin ADC_IN (TP130). If the AAF off box is selected the AAF filter is off and the ADC can be driven from ADC_IN.

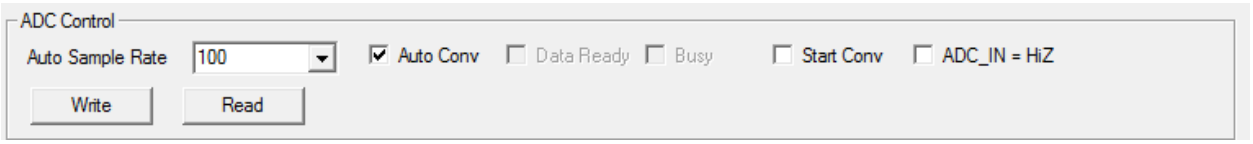


The AAF poles are set to nominally 00, 01, and 10 for 400, 2k or 10k in Hertz, respectively. Either one or both poles can be selected. The ADC sensitivity is set by adjusting the amplifier gain. The gain can be set to 10, 2 or 0.4.

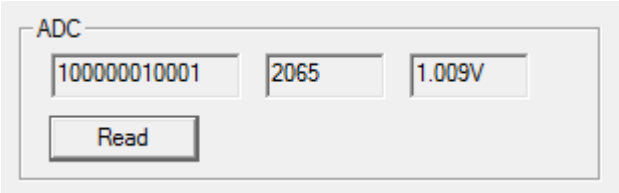
To allow operating room for the ADC (which operates from a 5V rail) the ADC_IN range is 0 to 2V. If an external input is to be sampled by the ADC, the internal circuitry driving the ADC_IN pin can be made high impedance by setting the Hi-Z bit in the ADC programming register.

ANALOG TO DIGITAL CONVERTER

The ADC uses a successive approximation register (SAR) design. The CLK input sequences the ADC logic. The Auto Sample Rate is set to multiples of the Sample Period (t_{SAMP}). This 3 bit N binary value sets the ADC auto sample rate = t_{SAMP} x $2^{N.}$. The ADC can be set to convert continuously (Auto Conv) or to convert on request using (Start Conv). Whenever a conversion is in process the Busy status bit is asserted. When the conversion is complete the Data Ready bit is set. The ADC value registers are updated when the Data Ready bit is asserted, but will not change during the process of a data read which starts by reading the upper byte and ends by reading the lower byte. If you select the Read button the Data Ready or Busy will display.

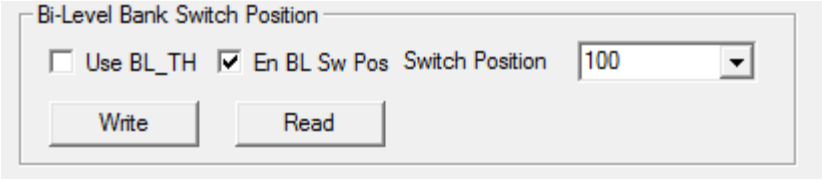


The ADC window will display the result of the latest conversion when the Read button is selected.

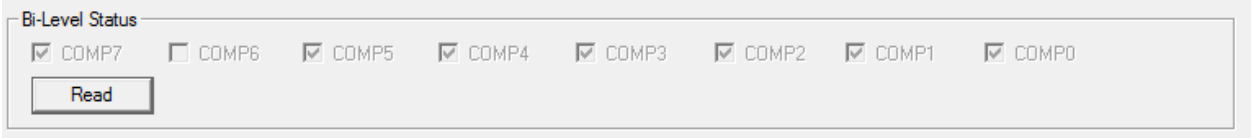


BI-LEVEL INPUTS

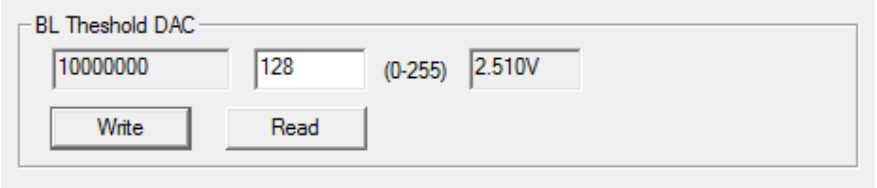
There are two sets of 8 bi-level inputs on the LX7730, first the 64 sensor inputs can be used as bi-level detection inputs. The Bi-level MUX and the AMUX are not independent; the En BL Sw Pos must be selected to use the Bi-Level MUX. The bi-level detection comparators monitor one position, simultaneously, from each of the input banks; the position is register selectable (bank 0 to 7, 000 to 111). See Sensor Multiplexer Block Diagram page 7. For example code 000 will connect CH1 to CH8 to the 8 bi-level comparators, and code 001 to CH9 to CH16 respectively. The comparators are sampled during the clock cycle that the Bi-Level Status is read, and the result placed in the Bi-Level Result Register shown in the GUI as Bi-Level Status.



The outputs of the group of 8 comparators available in this register are continuously updated and can be polled to monitor the status. The GUI allows you to see the status of the Bi-Level Result Register in the Bi-Level Status Window using the Read button. These functions are greyed-out because they cannot be selected but only show a change by the check mark appearing or disappearing.



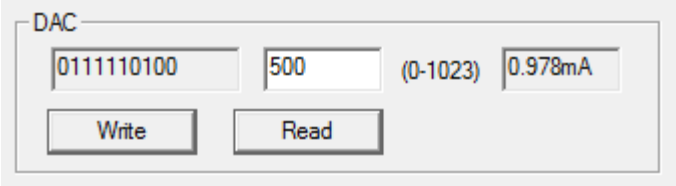
The selected eight bi-level inputs are compared to a common adjustable threshold that is developed using an 8 bit binary DAC.



In addition to these register based Bi-level comparators utilizing the Sensor inputs, the IC and the evaluation board includes 8 external Bi-level input pins (TP116 to TP123) that can be compared to either an internal 2.5V reference level or an external threshold voltage (BL_TH TP125) selected by checking the box Use BL_TH in the GUI. BLO1 to BLO8 are the comparator outputs of these 8 inputs (TP67 to TP83) and are referenced to VDD logic levels.

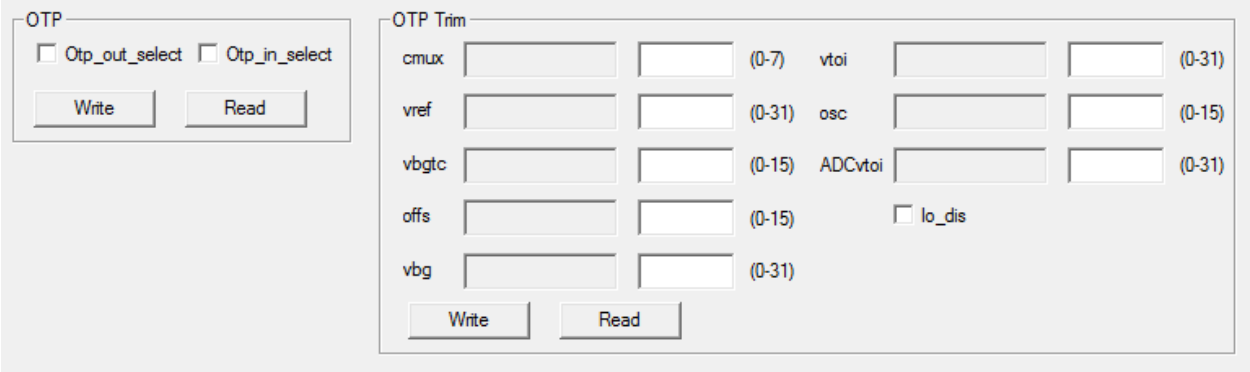
CURRENT DAC

The 10 bit ADC current source does not require recalibration. The output of the DAC should be terminated in a resistor that is less than 1.5kΩ to insure the DAC stays within its compliance range. A parallel 1nF or greater capacitor can also be used to help reduce bit change glitches. The DAC has complementary outputs that are accomplished by steering the current between the two outputs based on the DAC setting. At zero LSBs, the DAC_N is full scale and DAC_P is off. The Current DAC outputs are available at DAC_N (TP126) and DAC_P (TP127).



POWER & REFERENCE ADJUST (OTP)

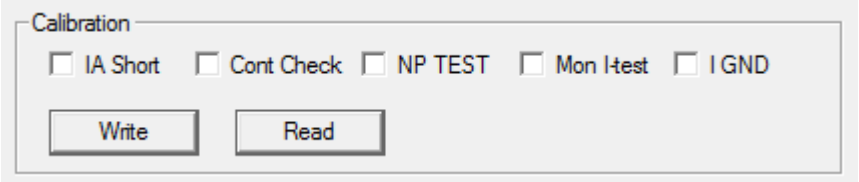
When Otp_out _select is checked and written to LX7730 the setting in the OTP trim boxes will override the default settings in the trimming register. These settings are temporary and must be re-written with a power cycle. If Otp_out_select is unchecked and Write pressed, the contents of the trim registers will revert back to the default values. If Otp_in_select is checked and written the default OTP bits are read into the display upon Read.



CALIBRATION

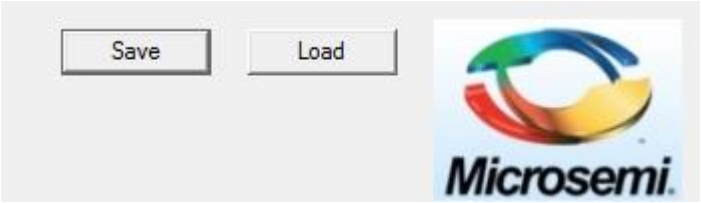
The Calibration buttons write to register 16 and is used to perform calibration of the amplifier offset and testing of the multiplexer switches and programmable current source multiplexer. For further details see the LX7730 datasheet which includes diagrams depicting the following modes.

Name	Default	Description
IA Short	0	If asserted, this action overrides the setting of the register of address 4 and causes a switch closure which shorts the inverting terminal of the instrumentation amplifier to the non-inverting terminal.
Cont Check	0	If selected, a current source is applied to the non-inverting input of the instrumentation amplifier. Current flows out of the AMUX to the selected CH# input pin. If the current encounters an open circuit in the AMUX or at the CH# pin, the voltage at the IA non-inverting pin will clamp. If the external sensor is properly attached, the voltage read by the ADC will include the impedance of the sensor plus the impedance of the two AMUX switches encountered in the current path
NP TEST	0	If selected, a current source is applied to the inverting input of the instrumentation amplifier and the non-inverting terminal is connected to VREF. Current flows out of the AMUX to the selected Inverting MUX CH# input pin. If the current encounters an open circuit in the AMUX or at the CH# pin, the voltage at the IA inverting pin will clamp. The Non-inverting terminal is connected to VREF_DIV for this test. If the external sensor is properly attached, the voltage read by the ADC will be the difference of VREF_DIV and the product of the current source and the impedance of the sensor plus the impedance of the two AMUX switches encountered in the current path. The impedance of the NP_MUX can be calculated once the other impedances are known using the CONT CHECK.
Mon I-test		Not Used.
I GND	0	If selected, this action overrides the setting of the register of address 4 and causes a switch closure which shorts the inverting terminal of the instrumentation amplifier to IC GND.

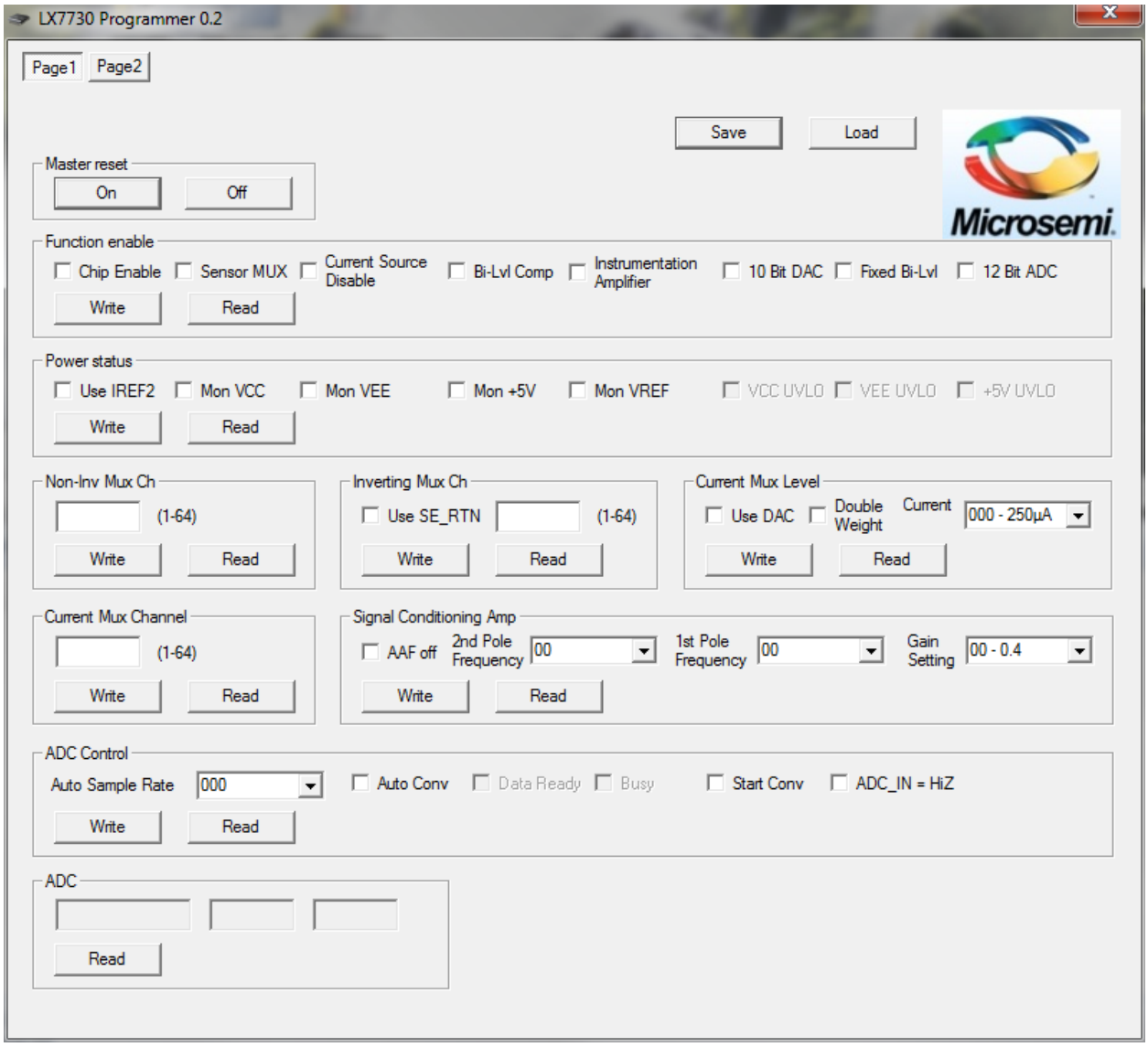


SAVE / LOAD

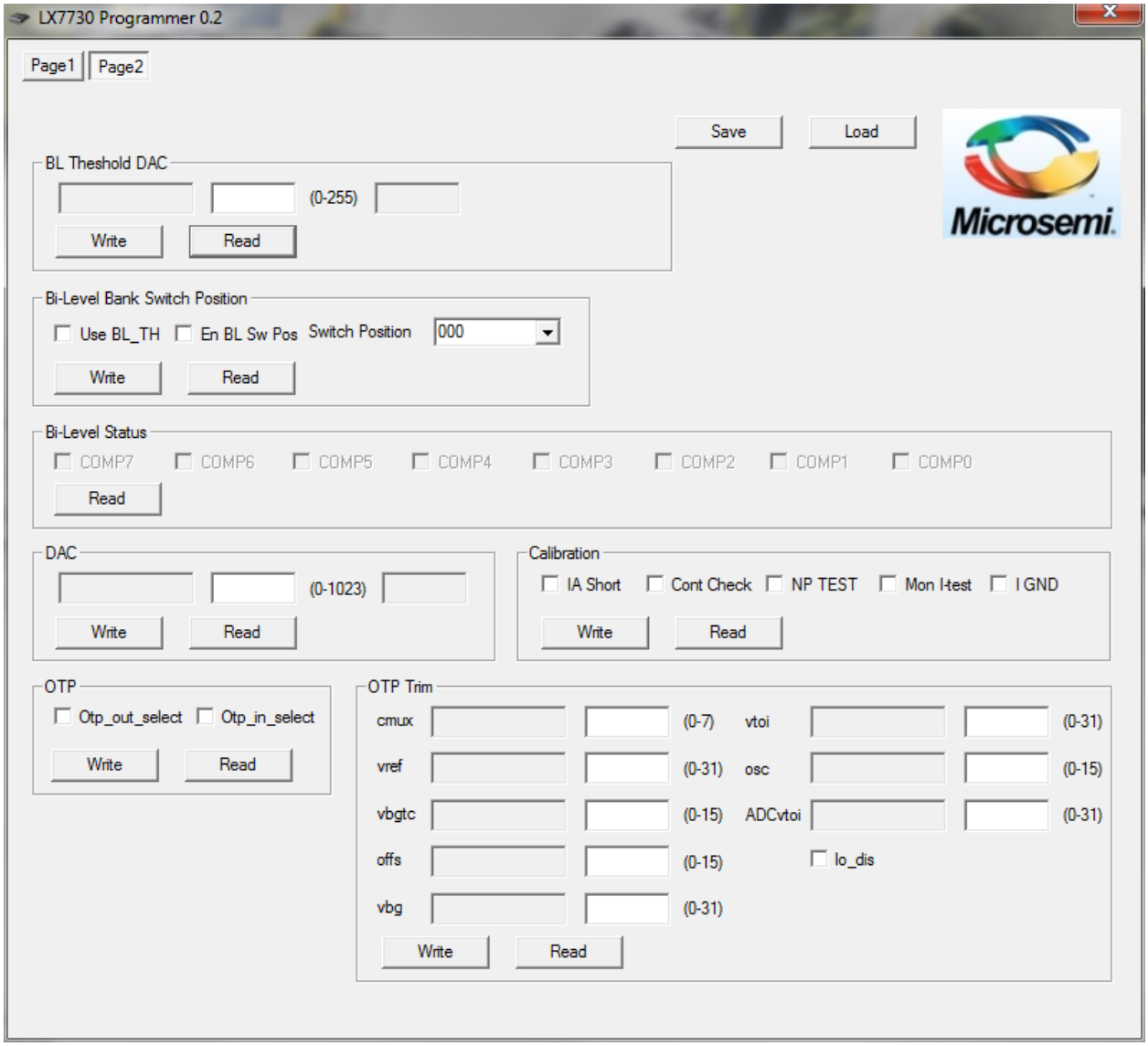
The SAVE / LOAD function allows the current settings of the GUI to be save to a txt file on your computer. You can restore a previous configuration by loading back this file and using the WRITE commands to restore each setting.

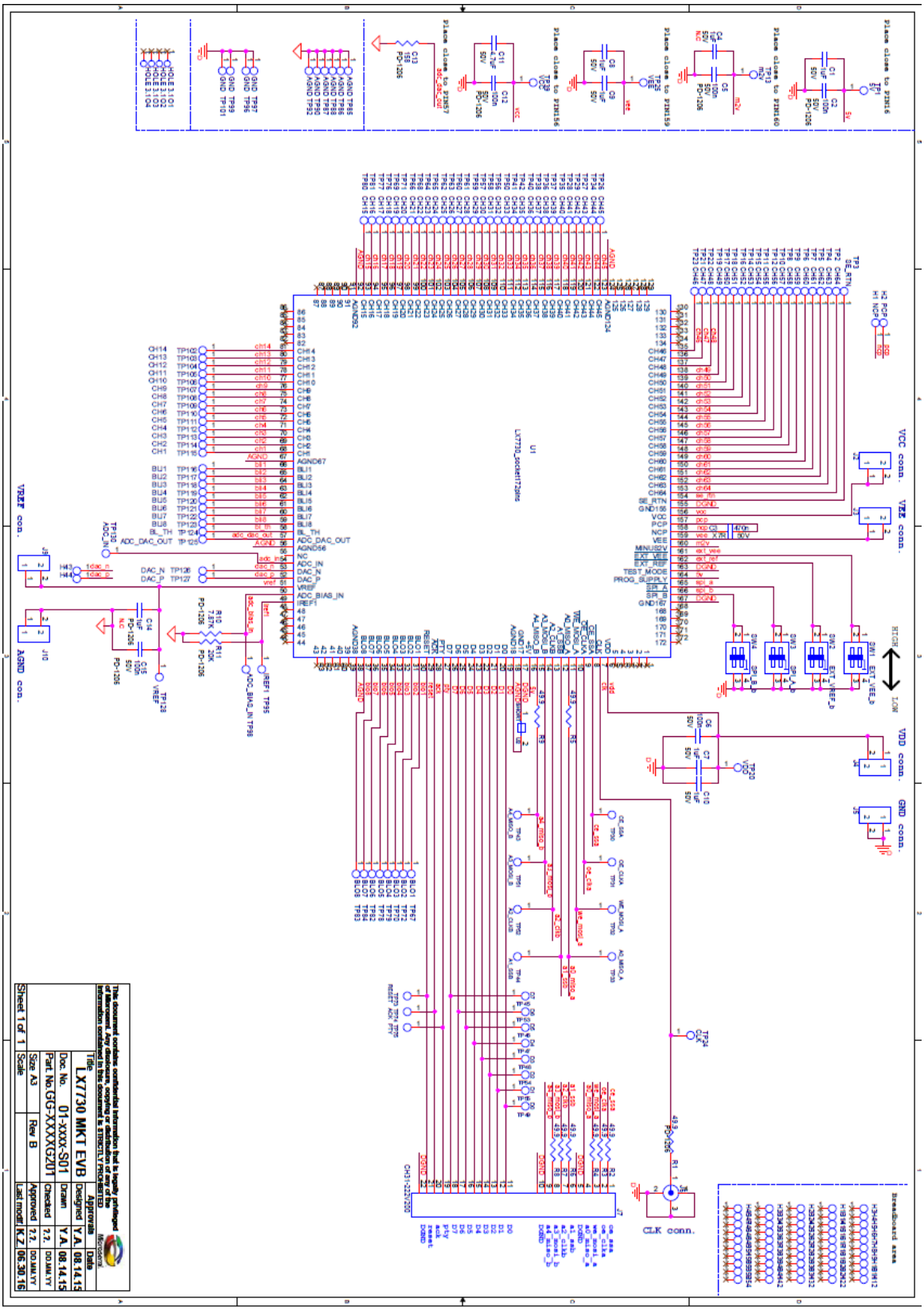


Programming Screen – Page 1



Programming Screen – Page 2




LX7730 MKT EVB
01-xxxx-S01
Part No:GS-XXXXXG2U1
Size A3
Rev B
Sheet 1 of 1
Scale
Last modif K.Z 06.30.16
Designed Y.A. 08.14.15
Drawn Y.A. 08.14.15
Checked Y.Z.
Approved Y.Z.
Approvals
Date
Title
Microsemi
This document contains confidential information that is legally privileged or Microsemi. Any disclosure, copying or distribution of any of the information contained in this document is STRICTLY PROHIBITED
U1
LX7730_socket172pins
VCC conn.
VREF conn.
VDD conn.
GND conn.
AGND conn.
CLK conn.
ADC_DAC_OUT
DAC_N
DAC_P
ADC_BIAS_IN
VREF
CLK
Breadboard area

Other Features of the Evaluation Board

+5V TP1

This pin is the low voltage power rail. It is generated internally using a linear regulator connected to the VCC rail. It is bypassed by C1 1µF and C2 100nF capacitors.

VREF TP126

+5V reference – This pin is a precision reference voltage that can be used to provide a voltage reference to sensors for precision measurements. It is bypassed by capacitors C14 1µF and C15 100nF to AGND. The internal reference can be disabled and an external reference connected to this pin; the internal voltage reference must be disabled in this case using the /EXT_REF programming pin SW2.

PARALLEL INTERFACE

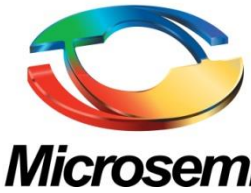
J7 pins 11 to 20 allow connection to the parallel interface these are logic I/O pins providing data bits, D0 (LSB) (pin 14) through D7 (pin 21. There is a weak pull-down on these pins.

J7 pin 19 provides the parity bit for the parallel data communication. Even parity is used for the combination of address and data bits and is used in both directions. There is a weak pull-down on this pin

J7 pin 20 is the acknowledge bit In the event of a parity error encountered in a serial or parallel data transfer, the /ACK pin is de-asserted (pulled high). It remains high until the start of the next data transfer logic sequence.

RESET

J7 pin 21 is the system reset logic input– This pin provides an external forced reset to the default state of all registers and flip-flops within the LX7730. A pulse width of greater than 500nS is required; there is a weak pull-down on this pin.



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