2.5/3.3V ECL Triple D Flip-Flop with Set and Reset

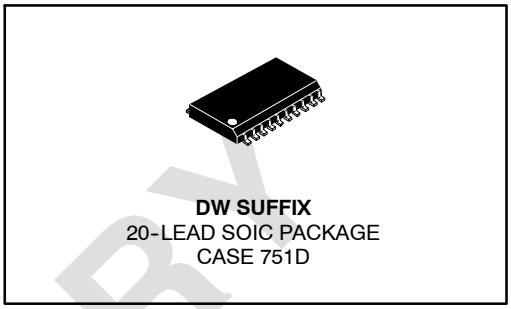
MC100ES6030

The MC100ES6030 is a triple master−slave D flip−flop with differential outputs. When the clock input is low, data enters the master latch and transfers to the slave during a positive transition on the clock input.

Each flip−flop has individual Reset inputs while the Set input is shared. The Set and Reset inputs are asynchronous and override the clock inputs.

Features

- 1.2 GHz minimum toggle frequency
- 450 ps typical propagation delay
- LVPECL operating range: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V
- LVECL operating range: V_{CC} = 0 V, V_{EE} = −2.375 V to −3.8 V
- 20−lead SOIC package
- Ambient temperature range −40°C to +85°C



DW SUFFIX
20−LEAD SOIC PACKAGE
CASE 751D

ORDERING INFORMATION

Device	Package
MC100ES6030DW	SO−20
MC100ES6030DWR2	SO−20

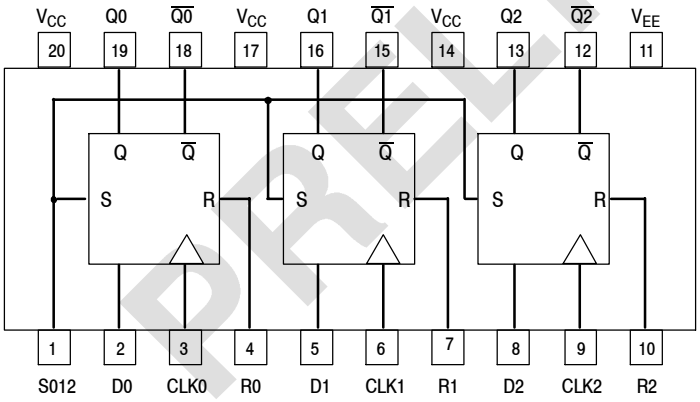


Figure 1. 20−Lead Pinout (Top View) and Logic Diagram

PIN DESCRIPTION

PIN	FUNCTION
D0−D2	ECL Data Inputs
R0−R2	ECL Reset Inputs
CLK0−CLK2	ECL Clock Inputs
S012	ECL Common Set Input
Q0−Q2, $\overline{Q0}$−$\overline{Q2}$	ECL Differential Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

R	S	D	CLK	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don't Care

Table 1. GENERAL SPECIFICATIONS

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model Charged Device Model	TBD TBD TBD
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 SOIC 500 LFPM, 20 SOIC	TBD TBD
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

Table 2. ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} - 0.3	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		-40 to +85	°C
T_{store}	Storage Temperature Range		-65 to +150	°C

a Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC CHARACTERISTICS (V_{CC} = 0 V, V_{EE} = -2.5 V ±5% or -3.8 V to -3.135 V; V_{CC} = 2.5 V ±5% or 3.135 V to 3.8 V, V_{EE} = 0 V)

		-40°C			0°C to 85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		TBD			TBD		mA
V_{OH}	Output HIGH Voltage[a]	V_{CC}-1085	V_{CC}-1005	V_{CC}-880	V_{CC}-1025	V_{CC}-955	V_{CC}-880	mV
V_{OL}	Output LOW Voltage[a]	V_{CC}-1830	V_{CC}-1695	V_{CC}-1555	V_{CC}-1810	V_{CC}-1705	V_{CC}-1620	mV
V_{IH}	Input HIGH Voltage	V_{CC}-1165		V_{CC}-880	V_{CC}-1165		V_{CC}-880	mV
V_{IL}	Input LOW Voltage	V_{CC}-1810		V_{CC}-1475	V_{CC}-1810		V_{CC}-1475	mV
I_{IN}	Input Current			±150			±150	µV

a Outputs are terminated through a 50Ω resistor to V_{CC}-2 volts. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported, but the power consumption of the device will increase.

Table 4. AC CHARACTERISTICS (V_{CC} = 0 V, V_{EE} = −2.5 V ±5% or −3.8 V to −3.135 V; V_{CC} = 2.5 V ±5% or 3.135 V to 3.8 V, V_{EE} = 0 V)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency	1.2			1.2			1.2			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK S, R					600					ps
t_s t_h	Setup Time Hold Time	150 200	0 100		150 200	0 100		150 200	0 100		ps ps
t_{RR}	Set/Reset Recovery	200	100		200	100		200	100		ps
t_{PW}	Minimum Pulse Width CLK S, R	400 650			400 650			400 650			ps ps
t_{JITTER}	Cycle−to−Cylce Jitter		< 2			< 2			< 2		ps
t_r/t_f	Output Rise/Fall Time (20%−80%)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

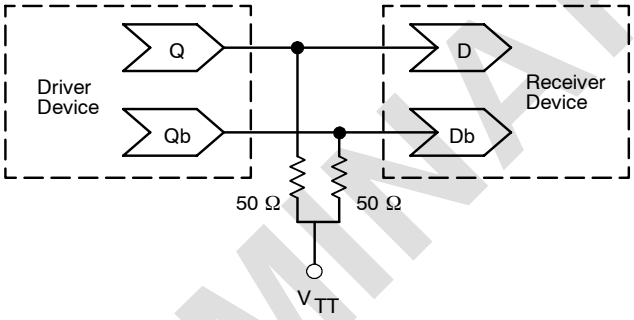
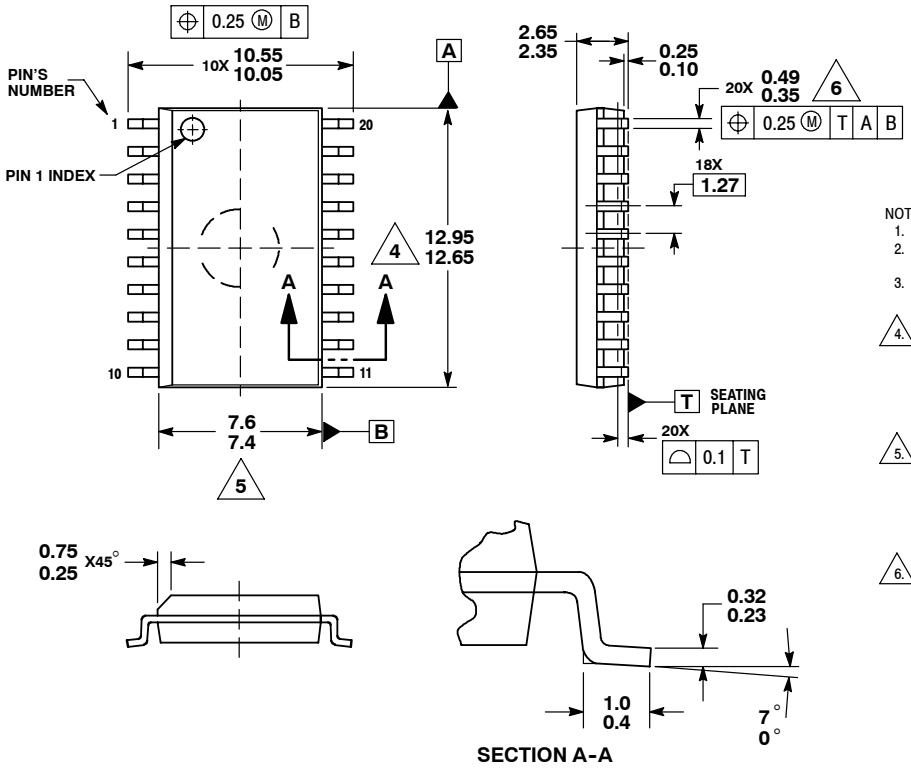


Figure 2. Typical Termination for Output Driver and Device Evaluation

OUTLINE DIMENSIONS

SOIC-20
DW SUFFIX
20 LEAD SOIC PACKAGE
CASE 751D-06
ISSUE H



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62mm.

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