AK4205

Ultra Low Noise and Distortion Headphone Amp with Analog Switch

1. General Description

The AK4205 is a stereo headphone amplifier corresponding to high resolution with built-in analog switch for Hi-Fi mobile. The AK4205 achieves industry's leading level ultra-low noise and ultra-low distortion characteristics (THD+N = -118dB).

The AK4205 is available in a small 36-pin QFN package. It can save the mounting area of the board by including resistors for gain adjustment and low-pass filter.

Application:

- **Smartphone**
- **Portable AMP**
- **Digital Media Player**
- **USB DAC**

2. Features

1. **Headphone Amplifier**
   - **Full-differential Input**
   - **Built-in Resistors for Gain Adjustment: Fixed to +0.5 dB @1 kHz**
   - **2nd order Low-pass Filter**
   - **Ultra-Low Noise: S/N 124dB**
   - **Ultra-Low Distortion: THD+N -118 dB @32 Ω, 34 mW**
     THD+N -120 dB @600 Ω, 6.7 mW
2. **Analog Switch**
   - **Selector Switch for Hi-Fi Audio path and Auxiliary path**
   - **Ultra-Low Distortion: THD -124dB@32 Ω, 34 mW**
   - **2 Vrms Output**
   - **Pop & Click Noise Free Switching Control**
   - **Built-in Negative Voltage Generator**
   - **Mute Function**
3. **Ta = –40 ~ 85°C**
4. **Power Supply:**
   - **Positive Power Supply (PVDDA, PVDDB): 6.0 V (typ)**
   - **Negative Power Supply (PVEEA, PVEEB): -5.0 V (typ)**
   - **Reference Power Supply (RVDD): 6.0 V (typ)**
   - **Analog Switch Power Supply (SWVDD): 3.3 V (typ)**
5. **Package:**
   - **36-pin QFN (5 x 5 mm, 0.4 mm pitch)**

3. Table of Contents

4. Block Diagram

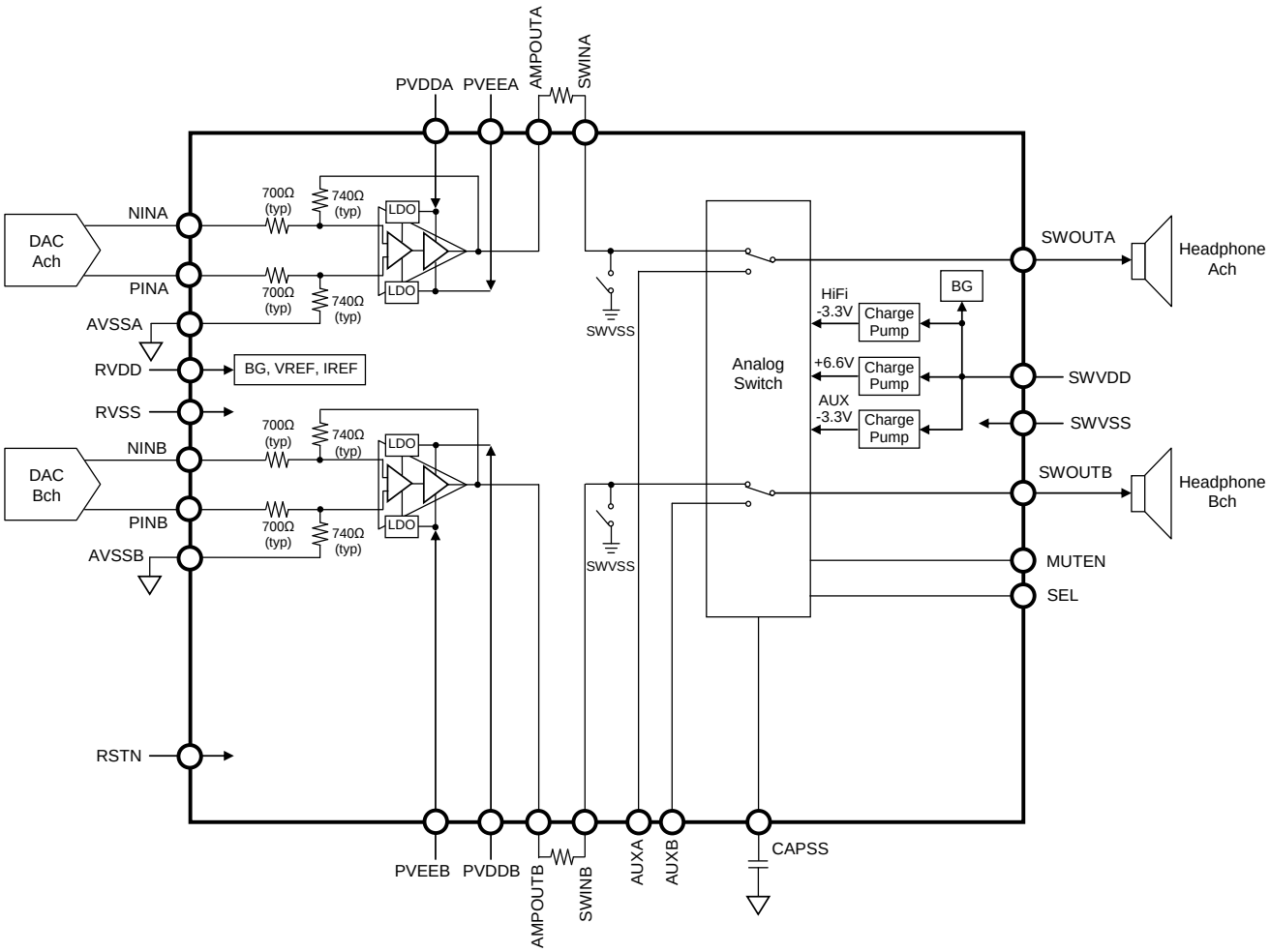


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations

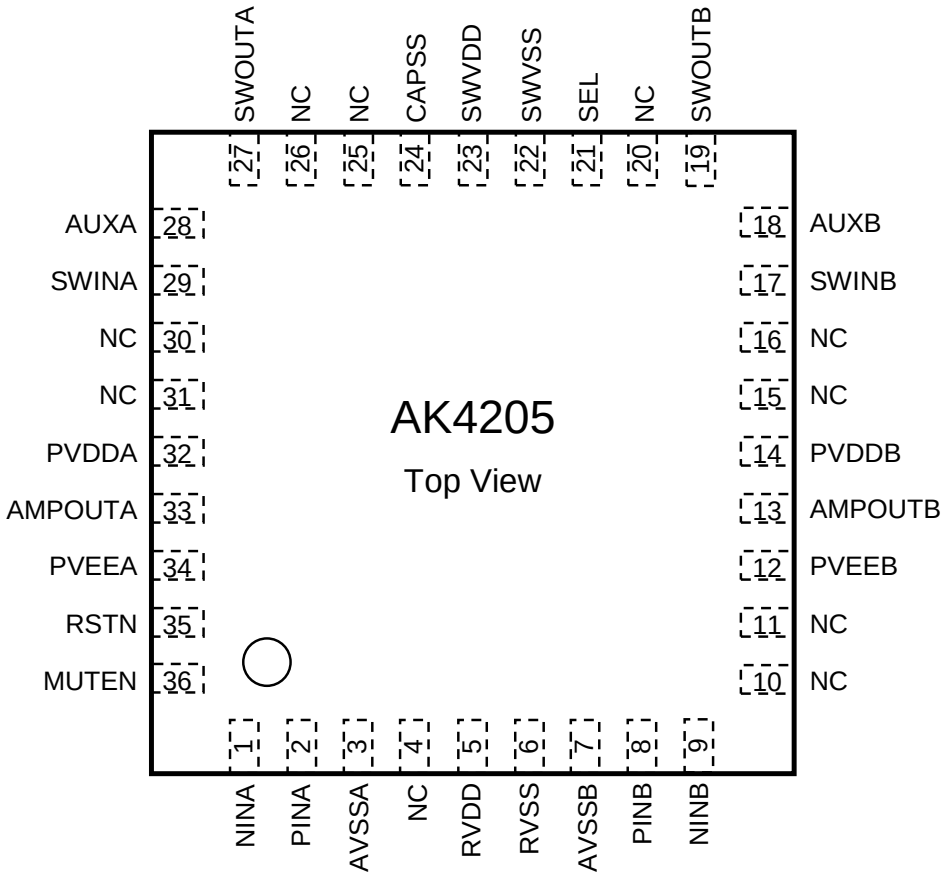


Figure 2. Pin Configurations

■ **Pin Functions**

No.	Pin Name	I/O	Function
1	NINA	I	Negative Analog Input A Pin
2	PINA	I	Positive Analog Input A Pin
3	AVSSA	-	Analog Ground A Pin
4	NC	-	No Connect pin. This pin should be connected to VSS.
5	RVDD	-	Reference Power Supply, 4.5 ~ 6.5 V
6	RVSS	-	Reference Ground Pin
7	AVSSB	-	Analog Ground B Pin
8	PINB	I	Positive Analog Input B Pin
9	NINB	I	Negative Analog Input B Pin
10	NC	-	No Connect pin. This pin should be connected to VSS.
11	NC	-	No Connect pin. This pin should be connected to VSS.
12	PVEEB	-	Headphone Amp Negative Power Supply B Pin, -4.5 ~ -5.5 V
13	AMPOUTB	O	Headphone Amp Output B Pin
14	PVDDB	-	Headphone Amp Positive Power Supply B Pin, 4.5 ~ 6.5 V
15	NC	-	No Connect pin. This pin should be connected to VSS.
16	NC	-	No Connect pin. This pin should be connected to VSS.
17	SWINB	I	HiFi Path Switch Input B Pin
18	AUXB	I	AUX Path Switch Input B Pin
19	SWOUTB	O	Switch Output B Pin
20	NC	-	No Connect pin. This pin should be connected to VSS.
21	SEL	I	HiFi/AUX Path Select Pin "H": HiFi Path (SWINA/B pins), "L": AUX Path (AUXA/B pins)
22	SWVSS	-	Switch Ground Pin
23	SWVDD	-	Switch Power Supply Pin, 3.0 ~ 3.6 V
24	CAPSS	O	Soft Start Capacitor Terminal Pin
25	NC	-	No Connect pin. This pin should be connected to VSS.
26	NC	-	No Connect pin. This pin should be connected to VSS.
27	SWOUTA	O	Switch Output A Pin
28	AUXA	I	AUX Path Switch Input A Pin
29	SWINA	I	Hi-Fi Path Switch Input A Pin
30	NC	-	No Connect pin. This pin should be connected to VSS.
31	NC	-	No Connect pin. This pin should be connected to VSS.
32	PVDDA	-	Headphone-Amp Positive Power Supply A Pin, 4.5 ~ 6.5 V
33	AMPOUTA	O	Headphone-Amp Output A Pin
34	PVEEA	-	Headphone-Amp Negative Power Supply A Pin, -4.5 ~ -5.5 V
35	RSTN	I	Reset Pin When "L", the AK4205 is held in reset. The AK4205 must be always reset upon power-up.
36	MUTEN	I	Mute Control pin "H": Normal Operation "L": SWOUTA and SWOUTB pins are mute state.
	Exposed Pad	-	The exposed pad on the bottom surface of the package should be connected to VSS. (Note 2)

Note 1. All digital input pins (SEL, RSTN, MUTEN pins) expect analog input/output pins (NINA, PINA, PINB, NINB, SWINB, AUXB, AUXA, SWINA) should not be left floating. I/O pins should be processed appropriately.

Note 2. Exposed Pad is not connected to VSS internally.

6. Absolute Maximum Ratings

(AVSSA=AVSSB=RVSS=SWVSS=0V; Note 3)

Parameter			Symbol	Min.	Max.	Unit
Power Supplies	Headphone Positive		RVDD PVDDA PVDDB	−0.3	7.0	V
	Headphone Negative		PVEEA PVEEB	−6.0	0.3	V
	Switch		SWVDD	−0.3	4.0	V
Input Current		(Note 4)	IIN1	-	±10	mA
		(Note 5)	IIN2	-	±200	mA
Analog Input Voltage		(Note 6) (Note 7)	VINA1	−0.3	RVDD+0.3 or 7.0	V
		(Note 8) (Note 9)	VINA2	−3.1	SWVDD+0.3 or 4.0	V
		(Note 9) (Note 10)	VINA3	−0.3	SWVDD+0.3 or 4.0	V
Digital Input Voltage		(Note 9) (Note 11)	VIND	−0.3	SWVDD+0.3 or 4.0	V
Ambient Temperature (powered applied)			Ta	−40	85	°C
Storage Temperature			Tstg	−65	150	°C
Junction Temperature			Tj	-	125	°C
Maximum Power Dissipation (Note 12)			Pd	-	500	mW

Note 3. All voltages are with respect to ground.
AVSSA, AVSSB, RVSS and SWVSS must be connected to the same analog ground plane.
RVDD/PVDDA/PVDDB and PVEEA/PVEEB must be connected to the same analog power supplies each.
Note 4. Except RVDD, PVDDA, PVDDB, SWVDD, SWINA, SWINB, AUXA and AUXB pins
Note 5. SWINA, SWINB, AUXA and AUXB pins
Note 6. PINA, NINA, PINB and NINB pins
Note 7. The maximum value of VINA1 is (RVDD+0.3)V or 7.0V, whichever is lower.
Note 8. SWINA, SWINB, AUXA and AUXB pins at ON state
Note 9. The maximum value of VINA2, VINA3 and VIND is (SWVDD+0.3)V or 4.0V, whichever is lower.
Note 10. SWINA, SWINB, AUXA and AUXB pins at OFF state
Note 11. RSTN, SEL, MUTEN pins
Note 12. This value is the internal loss of the AK4205, excluding the consumption of external dumping resistance and headphone. The maximum allowable junction temperature of the AK4205 is 125 °C. The θja (Junction to Ambient) in JESD51-9(2p2s) is 39.6 °C/W, and the internal temperature rise is 0.5W × 39.6 = 19.8 °C.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSSA=AVSSB=RVSS=SWVSS=0V; Note 13)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 14)	Headphone Positive		RVDD PVDDA PVDDB	4.5	6.0	6.5	V
	Headphone Negative		PVEEA PVEEB	-5.5	-5.0	-4.5	V
	Switch		SWVDD	3.0	3.3	3.6	V
Damping Resistor			Rd	-	33	-	Ω
Bypass Capacitor (Note 15)		PVDDA	C_{PVDDA}	0.1	-	-	μF
		PVDDB	C_{PVDDB}	0.1	-	-	μF
		PVEEA	C_{PVEEA}	0.1	-	-	μF
		PVEEB	C_{PVEER}	0.1	-	-	μF
Input DC Bias Voltage		(Note 16)	V_{DC1}	-	2.5	-	V
		(Note 17)	V_{DC2}	-	0	-	V
		(Note 18)	V_{DC3}	-0.3	0	0.3	V
Load Resistance			RL	16	-	-	Ω
Load Capacitance			CL	-	-	780	pF

Note 13. All voltages are with respect to ground.

Note 14. Each of power supplies: RVDD, PVDDA, PVDDB, PVEEA and PVEEB should be started simultaneously with SWVDD or after SWVDD. In particular, in order to avoid output pop noise, turn on the power supply of RVDD, PVDDA, PVDDB, PVEEA and PVEEB after SWVDD is completely powered up. When SWVDD = ON, RVDD, PVDDA, PVDDB, PVEEA and PVEEB can be turned OFF. Refer to "■ Analog Switch Power-up/down Sequence" about power up/down sequence of each power supply.

Note 15. Place them as close as possible to the IC. Refer to "Example of Layout" about detail.

Note 16. PINA, NINA, PINB and NINB pins

Note 17. SWINA, SWINB, AUXA and AUXB pins at ON state

Note 18. SWINA, SWINB, AUXA and AUXB pins at OFF state

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

(Ta = 25 °C; PVDDA = PVDDB = RVDD = 6.0 V, PVEEA = PVEEB = -5.0 V, SWVDD = 3.3 V; AVSSA = AVSSB = RVSS = SWVSS = 0 V; Signal Frequency, Level =1 kHz, 2 Vrms; Measurement Bandwidth = 20 Hz ~ 20 kHz; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
HP-amp + Analog Switch: PINA-NINA, PINB-NINB pins (Full Differential Input) → AMPOUA, AMPOUB pins → SWINA, SWINB pins → SWOUTA, SWOUTB pins, Rd=33Ω, SEL pin = "H" (Figure 3)					
Input Resistance	PINA, PINB pins	1120	1400	1680	Ω
	NINA, NINB pins	560	700	840	Ω
Input Voltage (Note 19)	PINA, PINB, NINA, NINB pins	-	2.83	-	Vpp
Output Power					
SWOUTA, SWOUTB pins					
	RL = 16 Ω	-	30	-	mW
	RL = 32 Ω	32	34	36	mW
	RL = 600 Ω	6.3	6.7	7.0	mW
Cut-off Frequency (Note 20)		-	400	-	kHz
THD+N	RL = 32 Ω (Note 21)	-	-114	-	dB
	RL = 32 Ω (Note 22)	-	-118	-	dB
	RL = 600 Ω (Note 21)	-	-117	-	dB
	RL = 600 Ω (Note 22)	-	-120	-	dB
S/N (A-weighted) (Note 23)		115	123	-	dB
S/N (A-weighted) (Note 22)		115	124	-	dB
Interchannel Isolation	RL = 32 Ω	100	120	-	dB
Interchannel Gain Mismatch		-	0	0.4	dB

Note 19. Input signal is DC2.5 V.

Note 20. When the output level of 1 kHz is 0 dB, it is the frequency at which the output level becomes -3.0 dB.

Note 21. Measured by Audio Precision APx555.

Note 22. A value of IC itself, the AK4205. It does not include the noise of measuring instrument.

Note 23. Measured by Audio Precision SYS 2722.

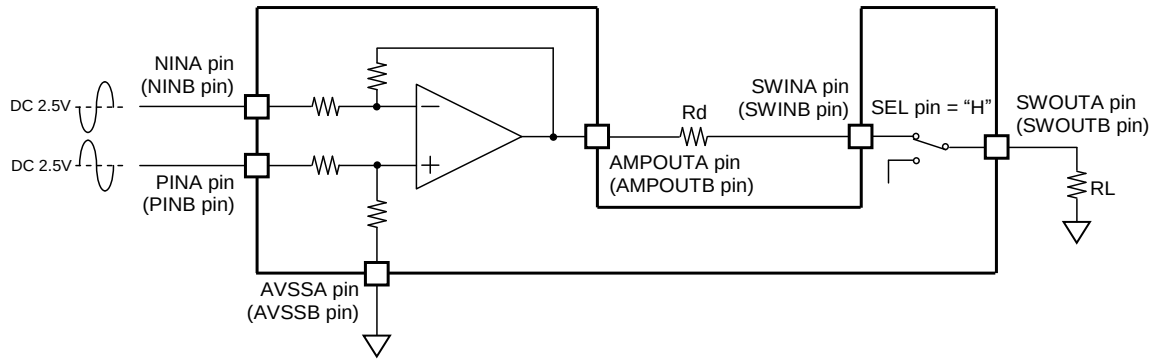


Figure 3. Measurement Circuit for HP-amp + Analog Switch

Parameter		Min.	Typ.	Max.	Unit
HP-amp Block: PINA-NINA, PINB-NINB pins (Full Differential Input) → AMPOUA, AMPOUB pins, Rd = 33Ω (Figure 4)					
Amp Gain	Gain Setting	0.18	0.48	0.78	dB
THD+N	RL = 32 Ω (Note 24)	-	-114	-	dB
	RL = 32 Ω (Note 25)	-	-118	-	dB
	RL = 600 Ω(Note 24)	-	-117	-	dB
	RL = 600 Ω(Note 25)	-	-120	-	dB
Output Noise Level (A-weighted) (Note 26, Note 27)		-	-116	-	dBV
Output Noise Level (A-weighted) (Note 25, Note 27)		-	-117	-	dBV
PSRR (Note 28)	f = 217 Hz	-	120	-	dB
	f = 1 kHz	-	115	-	dB

Note 24. Measured by Audio Precision APx 555. a
Note 25. A value of IC itself, the AK4205. It does not include the noise of measuring instrument.
Note 26. Measured by Audio Precision SYS 2722.
Note 27. Input signal is DC2.5 V
Note 28. When sine wave of 500 mVpp is superimposed on PVDDA, PVDDB, PVEEA, PVEEB.
Note 29. For analog characteristics of the headphone amplifier that is not listed in the above column, refer to the analog characteristics of the headphone amplifier + Analog Switch part.
Note 30. When only using the headphone amplifier, the power supply voltage described in the recommended operating conditions should also be input to SWVDD

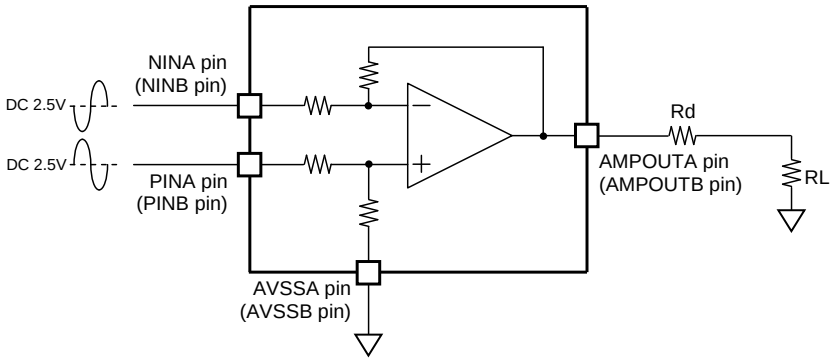
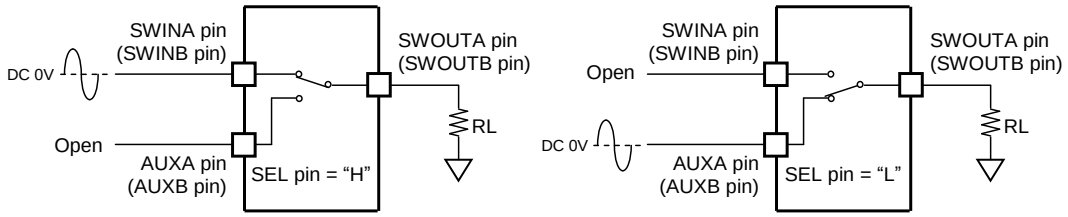


Figure 4. Measurement Circuit for Headphone-amp

Parameter			Min.	Typ.	Max.	Unit
Analog Switch Block: SWINA, SWINB pins (Single-ended Input) or AUXA, AUXB pins (Single-ended Input) → SWOUTA, SWOUTB pins (Figure 5)						
Analog Signal Range		SWINA, SWINB pins	-	6.0	-	Vpp
		AUXA, AUXB pins	-	6.0	-	Vpp
ON-Resistance	Hi-Fi Mode (SEL pin = "H")		-	0.26	-	Ω
	AUX Mode (SEL pin = "L")		-	0.30	-	Ω
THD						
	Hi-Fi Mode (SEL pin = "H")	RL = 32 Ω @ 33 mW	-	-124	-	dB
		RL = 600 Ω @ 6.7 mW	-	-135	-	dB
	AUX Mode (SEL pin = "L")	RL = 32 Ω @ 33 mW	-	-114	-	dB
		RL = 600 Ω @ 6.7 mW	-	-135	-	dB
Inter-channel Isolation		RL = 32 Ω	-	130	-	dB
		RL = 600 Ω	-	120	-	dB
Off Isolation (Note 31, Figure 6)		AUX → Hi-Fi	100	124	-	dB
		Hi-Fi → AUX	100	118	-	dB
PSRR (Note 32)		f = 217 Hz	-	115	-	dB
		f = 1 kHz	-	115	-	dB

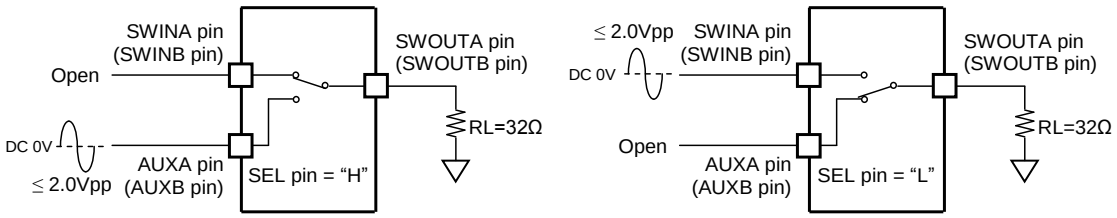
Note 31. The input signal to SWINA, SWINB, AUXA and AUXB pins is less than 2 Vpp (DC bias is 0 V, RL = 32 Ω.) The specification is shown in figure6.

Note 32. PSRR is applied to SWVDD with 500mVpp sine wave.



Hi-Fi mode (SEL pin = "H") AUX mode (SEL pin = "L")

Figure 5. Measurement Circuit for Analog Switch



AUX → Hi-Fi (SEL pin = "H") Hi-Fi → AUX (SEL pin = "L")

Figure 6. Measurement Circuit for Off Isolation

Parameter			Min.	Typ.	Max.	Unit
Power Supply Current:						
Power Up (All Circuit Power Up)						
	PVDDA+PVDDB (Quiescent, Iout = 0A)		-	5.4	11.5	mA
	PVEEA+PVEEB (Quiescent, Iout = 0A)		-	6.5	13.0	mA
	RVDD		-	2.0	3.0	mA
	SWVDD					
		RSTN pin = "H"	-	0.6	0.9	mA
		RSTN pin = "L"	-	200	300	μA

■ DC Characteristics

(Ta = -40 ~ 85 °C; PVDDA = PVDDB = RVDD = 4.5 V ~ 6.5 V, PVEEA = PVEEB = -4.5 V ~ -5.5 V, SWVDD = 3.0 V ~ 3.6 V; AVSSA = AVSSB = RVSS = SWVSS = 0 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
SEL, MUTEN, RSTN pins						
	High-Level Input Voltage	VIH	1.44	-	-	V
	Low-Level Input Voltage	VIL	-	-	0.36	V
	Input Rising Time	Tr			20	ns
	Input Falling Time	Tf			20	ns
	Input Leakage Current	Iin	-	-	0.5	μA
Output Voltage (CAPSS pin)	Hi-Fi Mode (SEL pin = "H")		2.37	2.5	2.63	V
	AUX Mode (SEL pin = "L")		1.3	1.4	1.5	V

■ Switching Characteristics

(Ta = -40 ~ 85 °C; PVDDA = PVDDB = RVDD = 4.5 V ~ 6.5 V, PVEEA = PVEEB = -4.5 V ~ -5.5 V, SWVDD = 3.0 V ~ 3.6 V; AVSSA = AVSSB = RVSS = SWVSS = 0 V)

Parameter (Figure 7)	Symbol	Min.	Typ.	Max.	Unit
Soft Start Timing (RL=32Ω,**Css=0.1μF:** Note 33**)**					
Turn-on Time	tON		59		ms
Turn-off Time	tOFF		29		ms
Turn-on slope (Vin = 20 mV)	tslON		1.0		V/s
Turn-off slope (offset Vin = 20 mV)	tslOFF		1.0		V/s
Reset Timing (RSTN pin: Note 33**)**					
RSTN Pulse Width (Css = 0.1 μF)	tRST	2	-	-	ms

Note 33. Css is a capacitor connected with the CAPSS pin.

■ Headphone-amp Power-up/down Timing

Parameter (Figure 9)	Symbol	Min.	Typ.	Max.	Unit
VDD Power up Slope (Note 34)	PUSLDD	-	-	15	mV/μs
VEE Power up Slope (Note 35)	PUSLEE	-50	-	-	mV/μs
VDD Power down Slope (Note 34, Note 36)	PDSLDD	-100	-	-	mV/μs
VEE Power down Slope (Note 35, Note 36)	PDSLEE	-	-	260	mV/μs
VDD-VEE non-overlap Time	tPU	0	-	-	ms
VEE-VDD non-overlap Time	tPD	0	-	-	ms

Note 34. RVDD, PVDDA, PVDDB pins

Note 35. PVEEA, PVEEB pins

Note 36. At power down, set the absolute value of the voltages of RVDD, PVDDA and PVDDB so that they do not fall below the absolute value of the voltage of PVEEA and PVEEB.

■ Timing Diagram

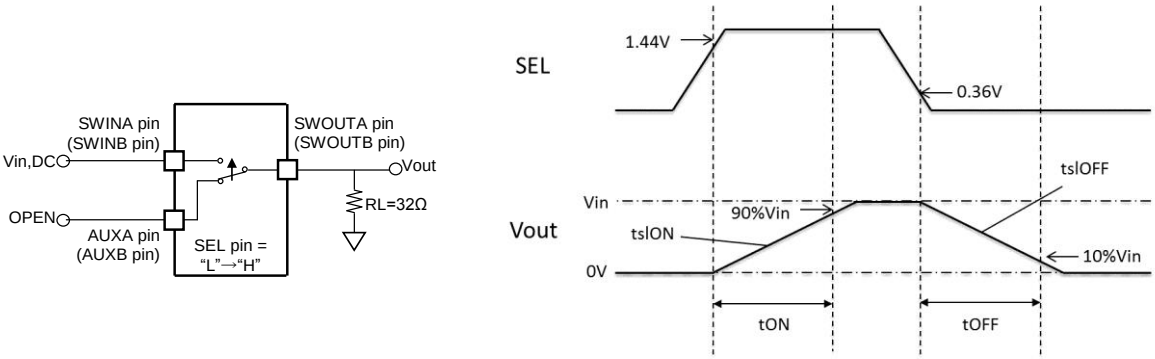


Figure 7. Soft Transition Timing

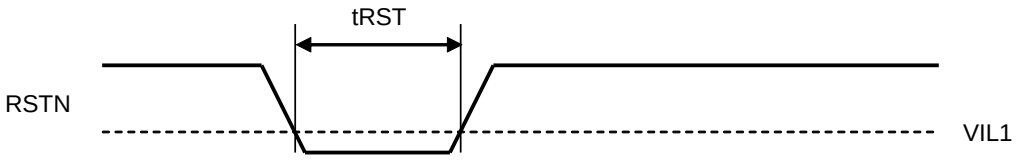


Figure 8. Reset Timing

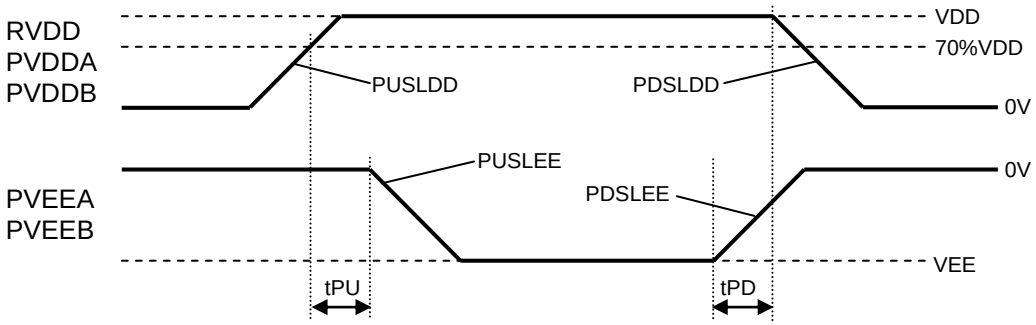


Figure 9. Headphone-amp Power-up/down Timing

9. Functional Descriptions

9.1 System Reset

Power supplies must be applied when the RSTN pin = “L”. Set the RSTN pin to “H” to release power-down after lapse of 1ms or longer from SWVDD power-up. The charge pump circuit starts to operate after the RSTN pin is set to “H”, and then the positive and negative voltage for analog switch are generated.

9.2 Charge Pump Circuit

The positive and negative powers are generated by built-in charge pump circuit from SWVDD voltage when RSTN pin = “H”. These generated powers are used for the analog switch. Input and output signals for the analog switch are single-ended and centered around on VSS (0V). The AK4205 has built-in capacitors for charge pump circuit; therefore no external capacitors are necessary.

The power-up time of the charge pump circuit is typ. 100μs (max. 500μs). The operating frequency of the charge pump circuit is depended on internal oscillator (typ. 4.5MHz). RVDD, PVDDA/B and PVEEA/B must be supplied after power-up the charge pump circuit.

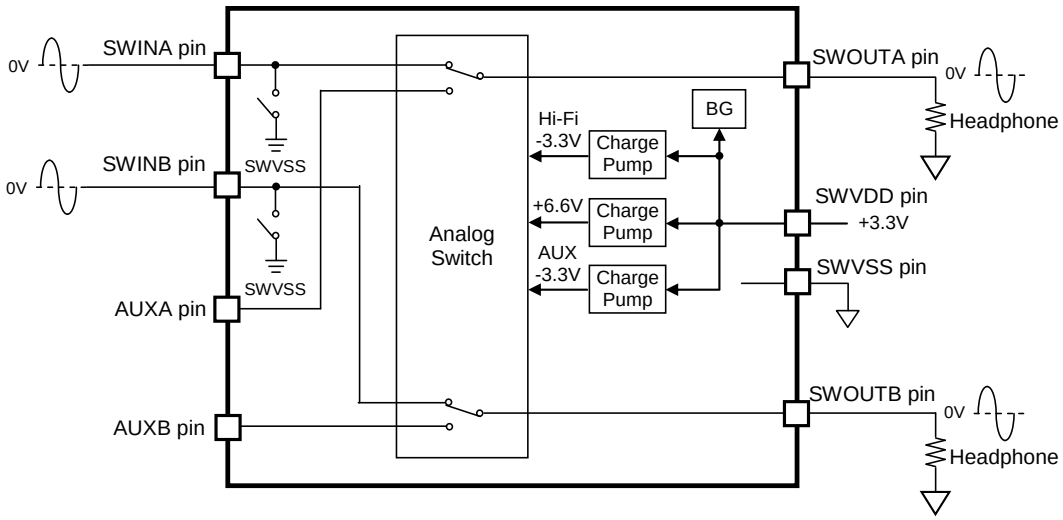


Figure 10. Charge Pump Circuit

9.3 Analog Switch & Mute Circuits

The AK4205 has an analog switch circuit with ultra-low on-resistance. It is able to achieve a 124 dB S/N(A-weighted) and -118dB THD+N when combined with a headphone amplifier that has ultra-low noise and distortion.

When the MUTEN pin = “H” and the SEL pin = “L”, the signals input to the AUXA and AUXB pins are output from the SWOUTA and SWOUTB pins, respectively. At this time, the SWINA and SWINB pins are pulled down to SWVSS by 4Ω (typ) resistance of SWA and SWB switches. When the MUTEN pin = “H” and the SEL pin = “H”, input signals to the SWINA and SWINB pins are output from the SWOUTA and SWOUTB pins, respectively. Soft mute transition is executed when changing the path (SEL pin = “L” → “H” or “H” → “L”) or when releasing a mute (MUTEN pin = “L” → “H”) to reduce pop noises. These transition times depend on the time constant of a capacitor that is connected to the CAPSS pin. Turn-off time will be 29ms (typ.) and Turn-on time will be 59ms (typ.) if the capacitor value Css = 0.1 μF

Setting of the SEL pin is ignored and the SWOUTA and the SWOUTB pins become mute state immediately by setting the MUTEN pin to “L”.

Table 1. Modes Control (x: Do not care)

MUTEN pin	SEL pin	Mode
L	x	Mute State (SWOUTA/B pins output Hi-Z)
H	L	AUX Mode (AUXA/B pins are enabled)
	H	Hi-Fi Mode (SWINA/B pins are enabled)

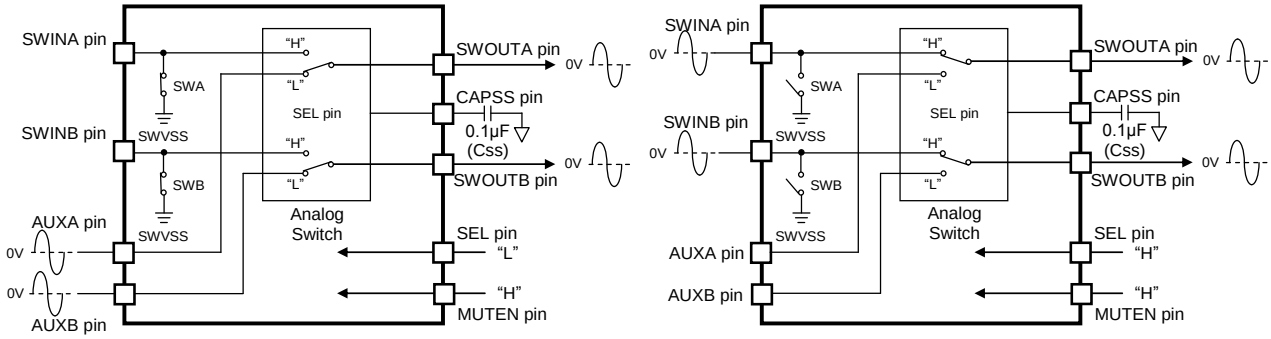


Figure 11. AUX Mode and Hi-Fi- Mode

9.4 Headphone Amplifier

Positive power of the internal headphone amplifier is supplied from the PVDDA/B pins and the negative power is supplied from the PVEEA/B pins. In these condition, AK4492 achieves -118dB THD+N.

The headphone outputs (AMPOUTA/B pins) are single-ended outputs centered around VSS (0 V) and DC cut capacitors are not necessary. A load resistance is 49 Ω (min.) including damping resistor (Rd). The headphone amplifier inputs should be fully differential inputs cantered at 2.5 Vpp DC bias voltage (PINA-NINA pins, PINB-NINB pins). The SWOUTA/B pin can output a 2Vrms when the input voltage PINB-NINA pins (PINB-NINB pins) = 2 Vrms, damping resistance (Rd) = 33 Ω and headphone load resistance (RL) = 600 Ω.

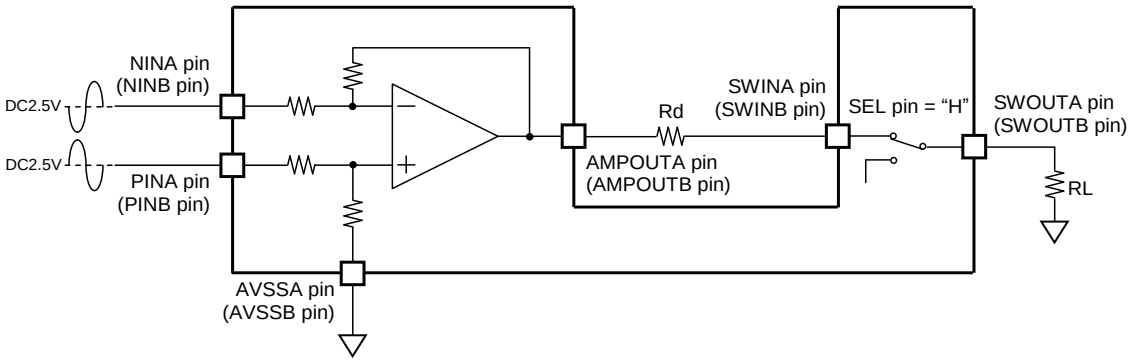


Figure 12. Headphone Amplifier

9.5 Control Sequence

■ Analog Switch Power-up/down Sequence

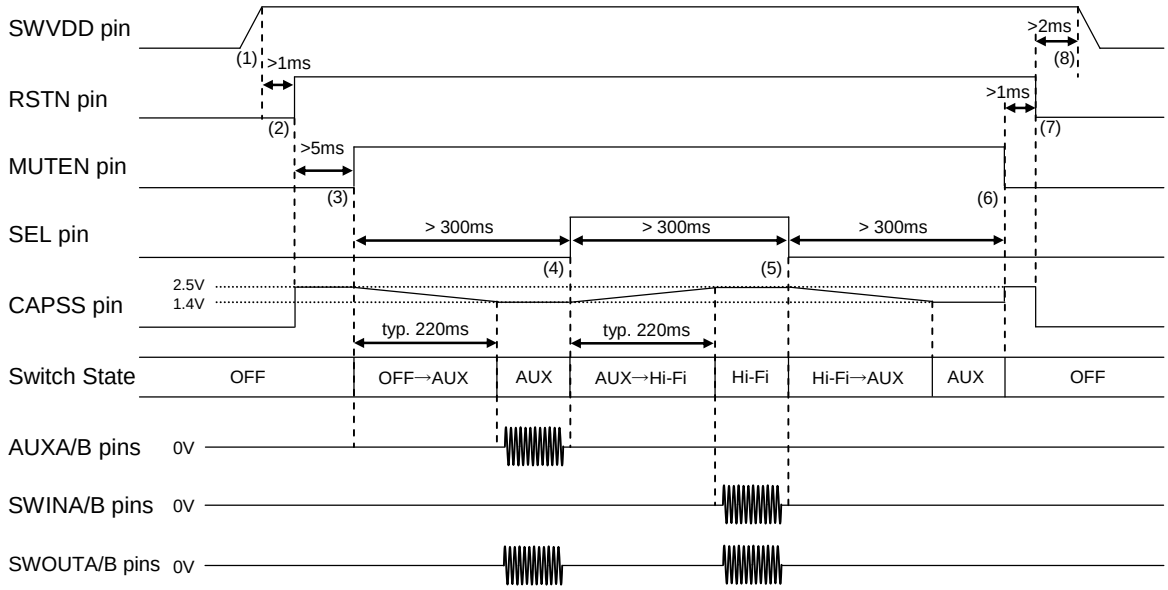


Figure 13. Power-Up/Down Sequence

<Power up Sequence>

(1) Power up SWVDD while the RSTN, SEL and MUTEN pins are all “L”.

(2) Set the RSTN pin “L” → “H” after power up SWVDD.
1 ms or more “L” period of the RSTN pin is necessary for a curtain reset of the AK4205.

(3) AUX Signal Output: MUTEN pin “L” → “H”
The analog switch near AUX side will be powered on gradually by setting the MUTEN pin to “H” after 5 ms from the reset release. Mute release time is determined by a capacitor connected to the CAPSS pin. For example, it will be 220 ms (typ.) if the capacitor value (Css) is 0.1 μF.

(4) Change to Hi-Fi Mode: SEL pin “L” → “H”
The data path is switched to Hi-Fi by setting the SEL pin = “H” after a lapse of 300 ms or more from the MUTEN pin = “H”. The SEL pin should be set to “H” after stopping the input of the AUXA/B pins. The transition time depend on the time constant of a capacitor that is connected to the CAPSS pin. It will be 220 ms (typ.) if the capacitor value (Css) is 0.1 μF.

Change to AUX Mode: SEL pin “H” → “L”
The data path is switched to AUX by setting the SEL pin = “L”. The SEL pin should be set to “L” after stopping the SWINA/B pins input. The transition time is determined by a capacitor connected to the CAPSS pin. For example, it will be 220 ms (typ.) if the capacitor value (Css) is 0.1 μF.

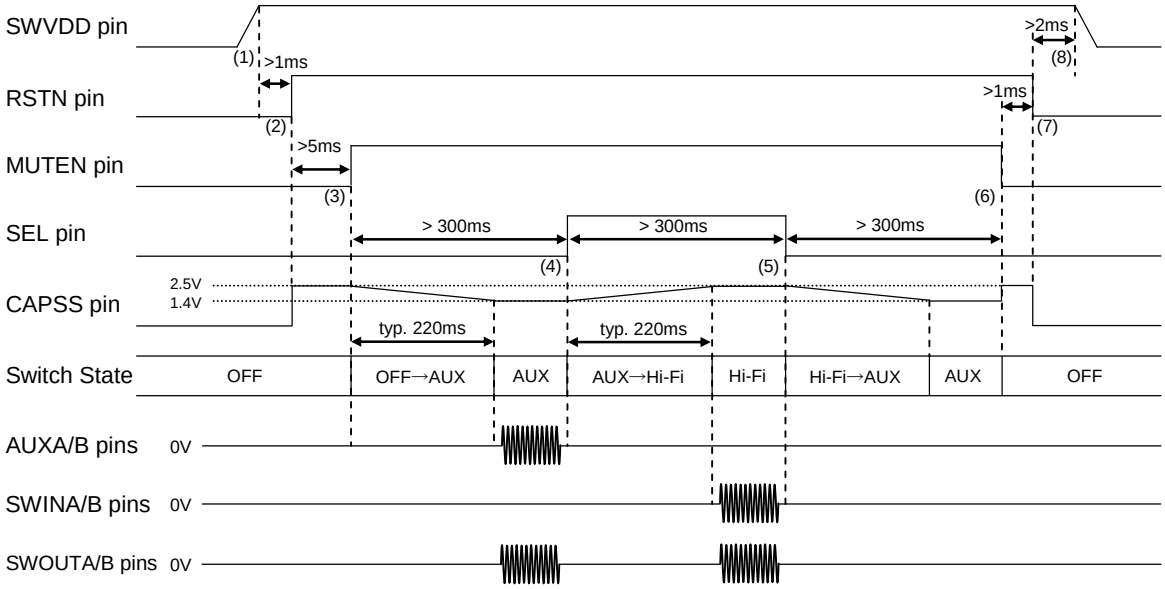


Figure 13. Power-Up/Down Sequence

<Power down Sequence>

(5) It is recommended that the data path is switched to AUX by setting the SEL pin = “L” to avoid pop noise in power down sequence.
(6) Stopping switch output: MUTEN pin “H” → “L”
When the MUTEN pin = "L", SWOUTA / B pins turns off momentarily. In order to avoid pop noise, set the MUTEN pin = "L" after 300 ms or more from the SEL pin = "L".
(7) After muting the output: RSTN pin “L” → “H”
After 1 ms from muting the output, set the RSTN pin to “L”.
(8) After 2 ms or more from the RSTN pin = "L", turn off SWVDD power supply.

■ Hi-Fi Mode ⇔ AUX Mode Pop Noiseless Change Sequence

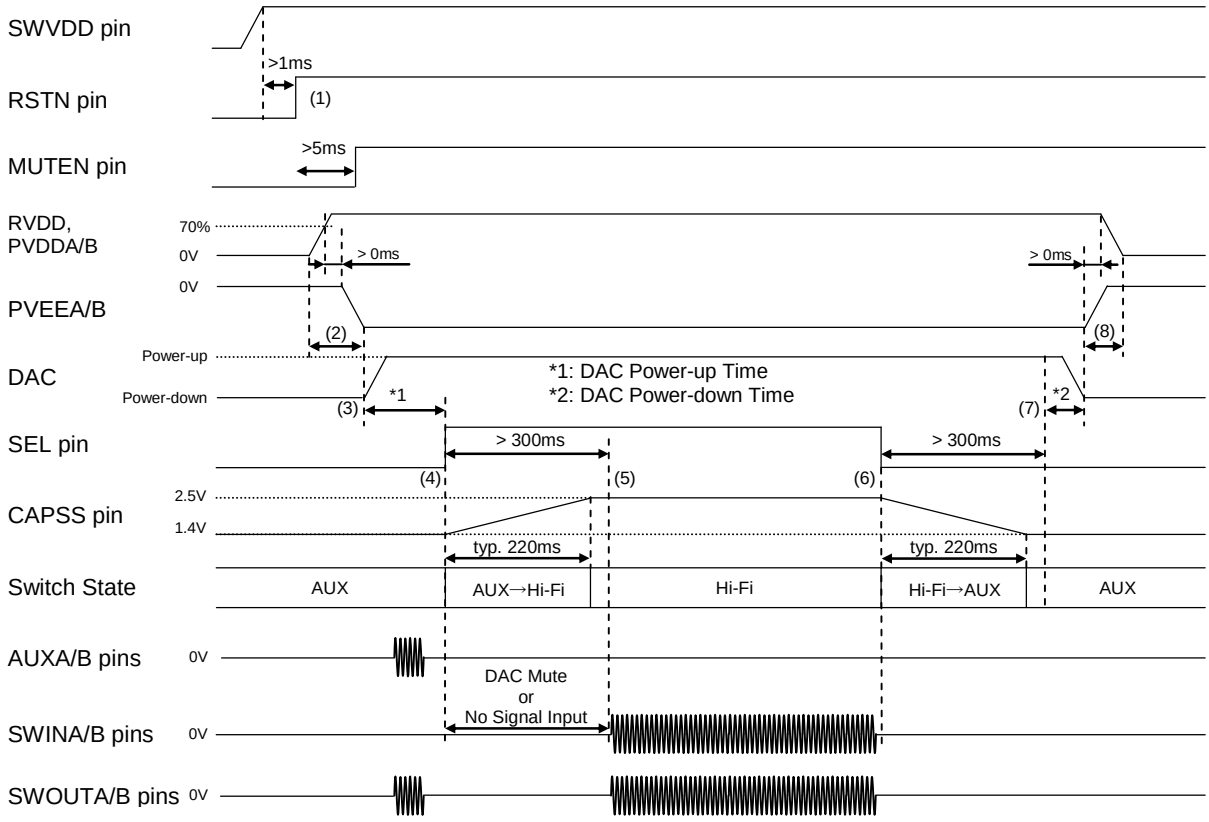


Figure 14. Hi-Fi ⇔ AUX Path Switching Sequence

<Sequence>

(1) At first, set up analog switch according to the its power-up/down sequence (Refer to "p16.■ Analog Switch Power-up/down Sequence (1)~(3)").

Changing AUX Mode ⇒ Hi-Fi Mode

(2) When the AUX input is 0V, power up headphone-amp power supplies (RVDD, PVDDA/B, PVEEA/B). After RVDD and PVDDA/B are powered up, power up PVEEA/B. (Refer to "p11.■ Headphone-amp Power-up/down Timing")
(3) When the headphone-amp is powered up, power up the power supply of DAC connected near Hi-Fi side.
(4) After DAC output is Enabled: SEL pin "L" → "H"
Do not input signal to the SWINA/B pins in the middle of transition.
(5) DAC signal starts being output.

Changing Hi-Fi Mode ⇒ AUX Mode

(6) Set the SEL pin "H" → "L" after stopping DAC output.
Set the SEL pin to "L" after the DAC is muted or data input is stopped.
(7) Power-up the DAC with an interval of 300ms or more after setting the SEL pin to "L".
(8) Turn off the headphone amplifier power supplies (PVEEA/B, RVDD, PVDDA/B) after power downing the DAC. PVEEA/B must be powered down before RVDD and PVDDA/B. (Refer to "p11.■ Headphone-amp Power-up/down Timing")

10. Recommended External Circuits

10.1. General Example of External Circuit

Figure 15 shows the system connection diagram. An evaluation board (AKD4205) is available for fast evaluation as well as suggestions for peripheral circuitry.

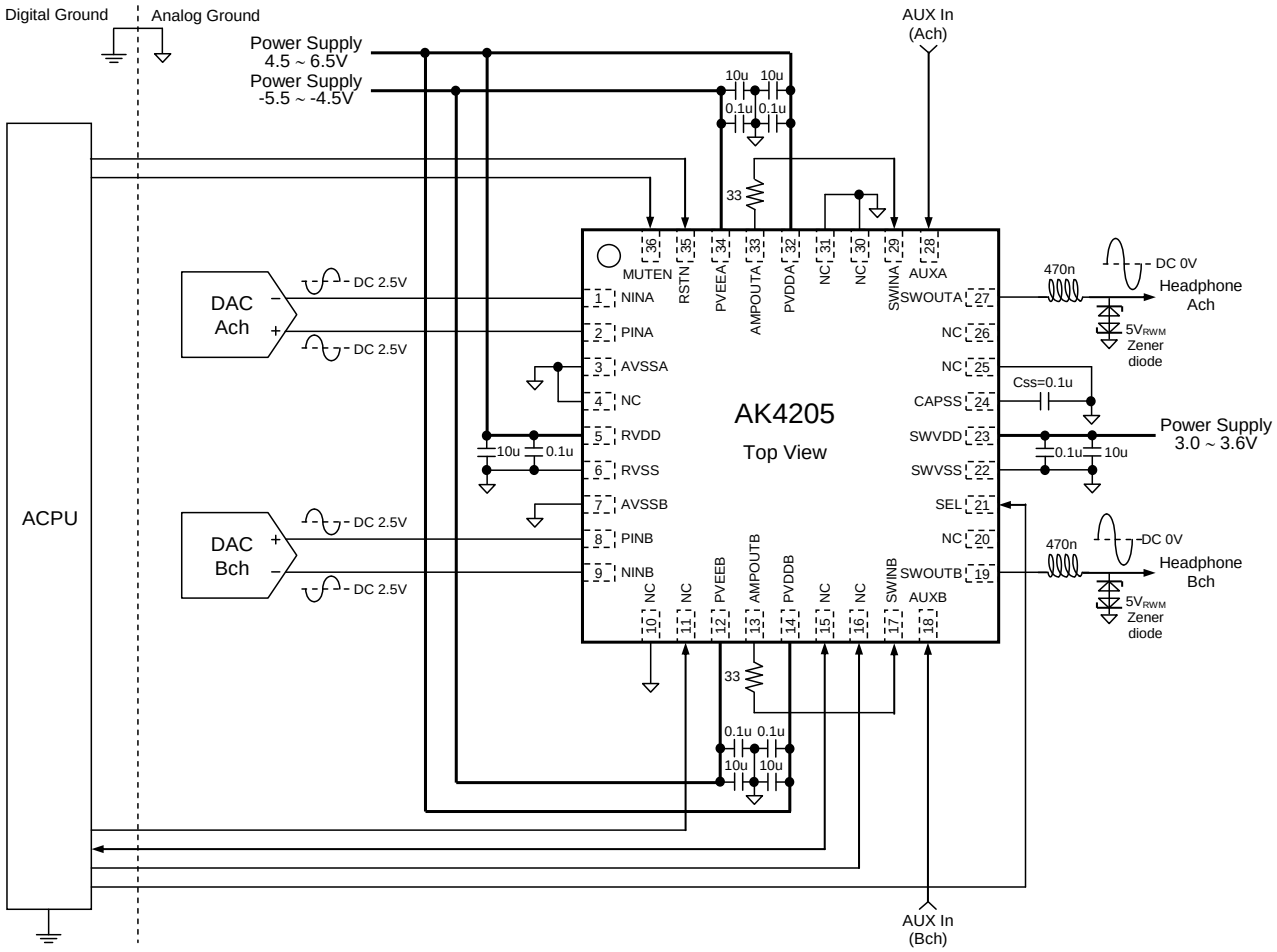


Figure 15. Circuit Example with AK4205

Note:

- RVSS, SWVSS, AVSSA and AVSSB of the AK4205 must be distributed separately from the ground of external controllers.
- AVSSA, AVSSB and headphone ground must be connected to the same analog ground plane to minimize contact impedance.
- The CAPSS pin should be connected to the ground with 0.1μF or more capacitor to minimize pop & click noise by switching path.
- It is recommended to connect inductors (typ. 470nF) between SWOUTA/B and headphone outputs, and zener diodes (V_{RWM} = 5V) between headphone outputs and the analog ground for a circuit design considering the IEX61000-4-2 standard.

1. Grounding and Power Supply Decoupling

The AK4205 requires careful attention to power supply and grounding arrangements. PVDDA, PVDDB, PVEEA, PVEEB and RVDD are usually supplied from the system's analog supply, and SWVDD is supplied from the system's another analog power supply. RVDD/PVDDA/PVDDB and PVEEA/PVEEB must be connected to the same analog power supplies each. The RSTN pin should be held "L" when power supplies are tuning on. The RSTN pin is allowed to be "H" after SWVDD is applied and settled.

In order to avoid the pop noise of SWOUTA and SWOUTB output at power-up/down, refer to "p16.■ Analog Switch Power-up/down Sequence"

RVSS, SWVSS, AVSSA, AVSSB and expose pad of the AK4205 should be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value bypass capacitor is to be closest.

2. Analog Inputs

The headphone amplifier inputs (PINA-NINA pins and PINB-NINB pins) support full-differential format. The input signal range is nominally typ. 2.83 Vpp, centered around 2.5 V. The analog switch inputs (SWINA, SWINB, AUXA and AUXB pins) support single-ended format. The input signal range is nominally typ. 6.0 Vpp, centered around VSS (0 V).

3. Analog Outputs

The headphone output (AMPOUTA and AMPOUTB pins) is single-ended and centered around VSS (0 V). There is no need for AC coupling capacitors. The AMPOUTA and AMPOUTB pins should be connected to SWINA and SWINB pins with a dumping resistor (Rd) in series. The analog switch output (SWOUTA and SWOUTB pins) is single-ended and centered around VSS (0 V), and they should be connected directly to a headphone. There is no need for AC coupling capacitors.

10.2 Example of the connection with AK4492

The AK4492 is a 32-bit 2ch Premium DAC. Ultra low distortion characteristics are realized by distortion reduction technology. The digital input supports up to 768 kHz PCM and 11.2 MHz DSD (Direct Stream Digital), making the AK4205 suitable for high-resolution sound source playback that is becoming popular with smart phones, audio players and etc.
A connection example with the AK4492 is shown below. VSS and DVSS should not interfere each other by the layout design.

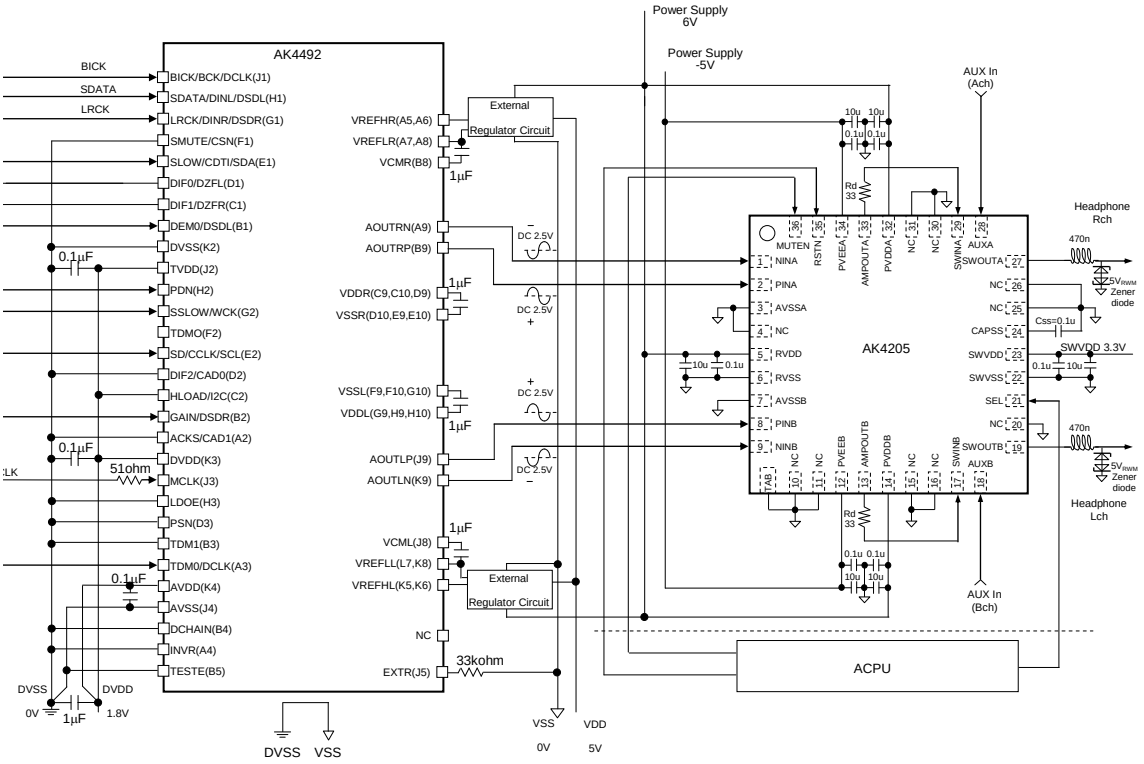


Figure 16. Circuit Example with AK4205 and AK4492

11. Example of Layout

Figure 17 shows the recommended layout of the AK4205.

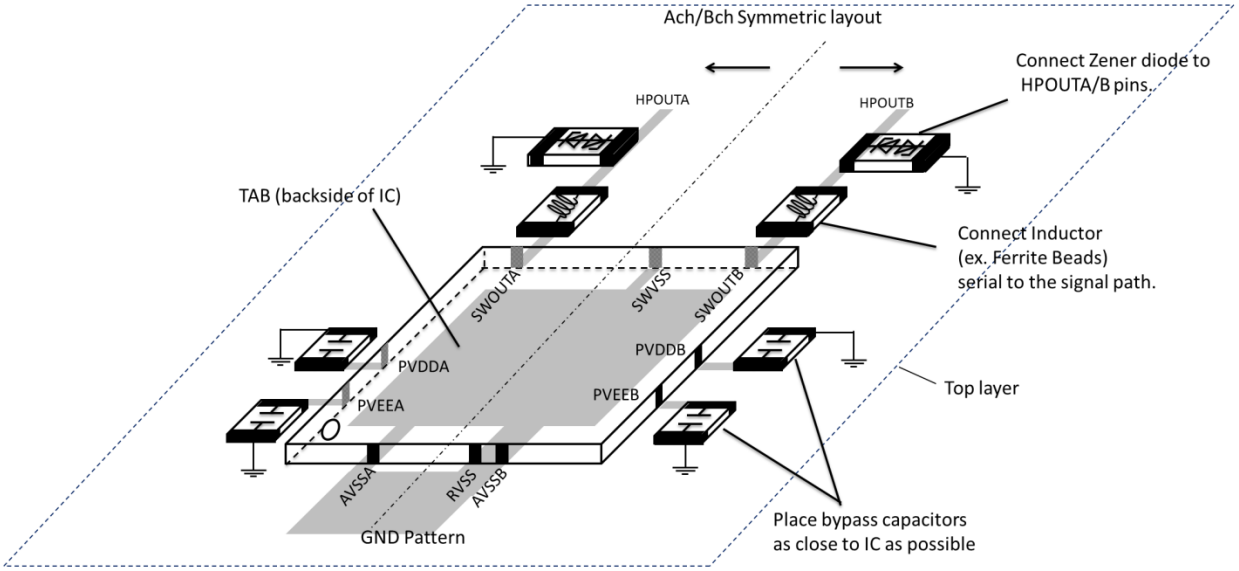


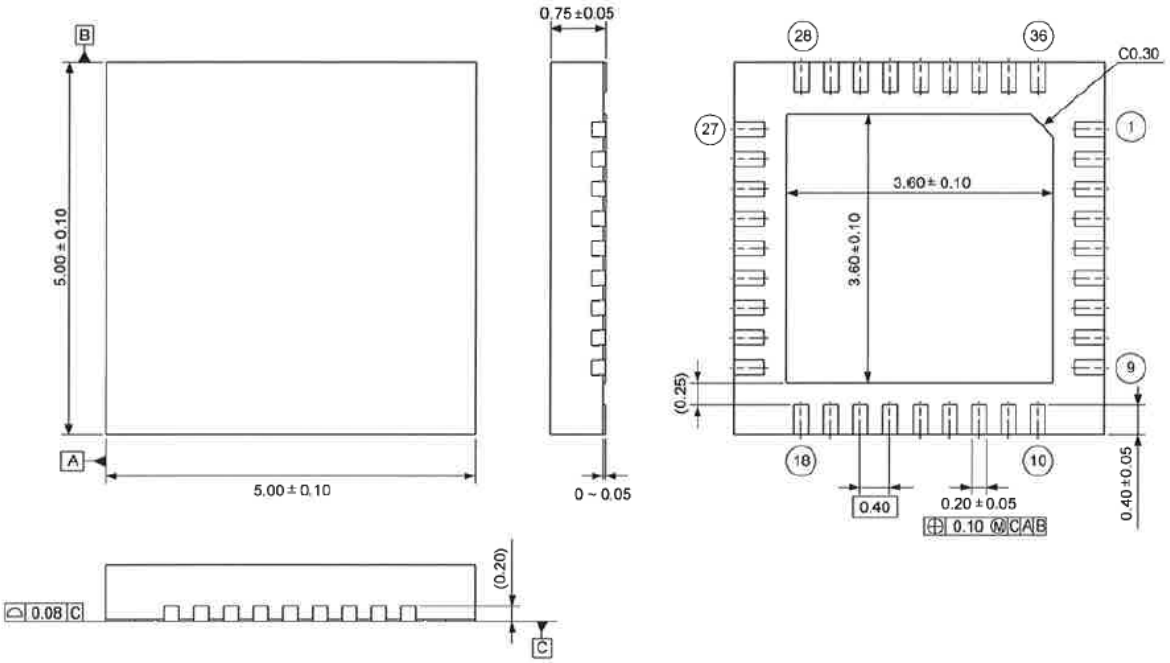
Figure 17. Recommended Layout Example of AK4205

Note:

- Connect AVSSA, AVSSB, RVSS, SWVSS and Exposed PAD (TAB) on the reverse side of the IC at the top layer and minimize the wiring impedance between each Pin as much as possible. When connected with VIA, the characteristics such as THD may deteriorate due to parasitic inductance.
- Place the Bypass Capacitor between PVDDA, PVDDB, PVEEA, PVEEB and GND in the immediate vicinity of the IC and minimize the wiring impedance as much as possible.
- For circuit design considering the IEC 61000-4-2 standard, it is recommended to connect an inductor (typ. 470 nF) between the SWOUTA/B terminal and the headphone output, and a zener diode (V_{RWM} = 5 V) between the headphone output and the analog ground.

12. Package

■ Outline Dimensions



* The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material & Lead finish

Package molding compound: Epoxy Resin, Halogen (Br and Cl) free
Lead frame material: Cu Alloy
Pin surface treatment: Solder (Pb free) plate (Sn100 %)

■ Marking

XXXXX: Date code (5 digits)
Pin #1 indication

13. Ordering Guide

■ **Ordering Guide**

AK4205EN -40 ~ +85°C 36-pin QFN

14. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
16/12/22	00	First Edition		

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