Ultralow Jitter Multioutput Clock Synthesizer with Integrated VCO

FEATURES

- **Low Noise Integer-N PLL with Integrated VCO**
- **Output Jitter:**
  - **90fs RMS (12kHz to 20MHz)**
  - **115fs RMS (ADC SNR Method)**
  - **Noise Floor = –165dBc/Hz at 250MHz**
- **EZSync™, ParallelSync™ Multichip Synchronization**
- **SYSREF Generation for JESD204B, Subclass 1**
- **Output Frequency Range:**
  - **1.95MHz to 2.5GHz (LTC6951)**
  - **2.1MHz to 2.7GHz (LTC6951-1)**
- –229dBc/Hz Normalized In-Band Phase Noise Floor
- –277dBc/Hz Normalized In-Band 1/f Noise
- Five Independent, Low Noise Outputs
- Reference Input Frequency up to 425MHz
- LTC6951Wizard™ Software Design Tool Support
- –40°C to 105°C Operating Junction Temperature Range

APPLICATIONS

- High Performance Data Converter Clocking
- Wireless Infrastructure
- Test and Measurement

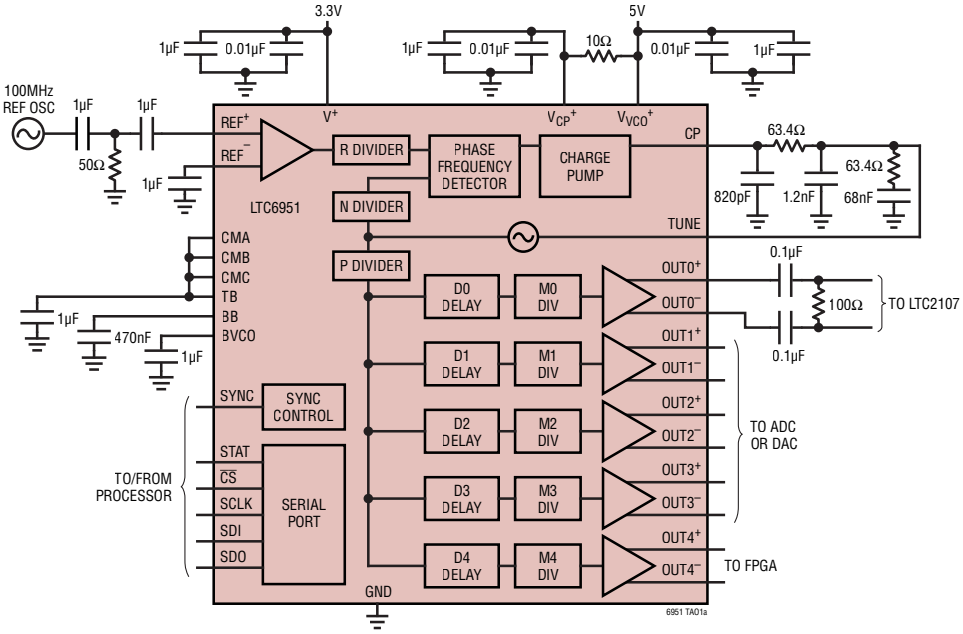
DESCRIPTION

The LTC®6951 is a high performance, low noise, Phase Locked Loop (PLL) with a fully integrated VCO. The low noise VCO uses no external components and is internally calibrated to the correct output frequency with no external system support.

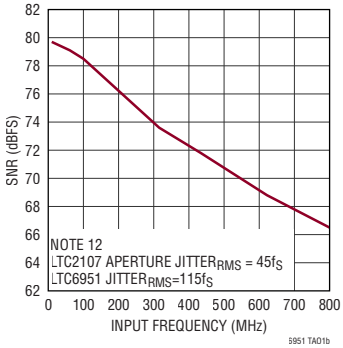
The clock generation section provides five outputs based on the VCO prescaler signal with individual dividers for each output. Four outputs feature very low noise, low skew CML logic. The fifth output is low noise LVDS. All outputs can be synchronized and set to precise phase alignment using the programmable delays.

Choose the LTC6951-1 if any desired output frequency falls in the ranges 2.5GHz to 2.7GHz, 1.66GHz to 1.8GHz, or 1.25GHz to 1.35GHz. Choose the LTC6951 for all other frequencies.

TYPICAL APPLICATION



SNR vs Input Frequency of LTC6951 Clocking an LTC2107, f_S = 210Msps, A_{IN} = –3dBFS



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

V^+ (V_{REF}^+, V_{RF}^+, V_D^+, V_{OUT}^+) to GND 3.6V

V_{CP}^+, V_{VCO}^+ to GND 5.5V

Voltage on CP Pin ..... GND – 0.3V to V_{CP}^+ + 0.3V

Voltage on all other Pins ..... GND – 0.3V to V^+ + 0.3V

Current into $OUTx^+$, $OUTx^-$, (x = 0, 1, 2, 3, 4) ..... ±25mA

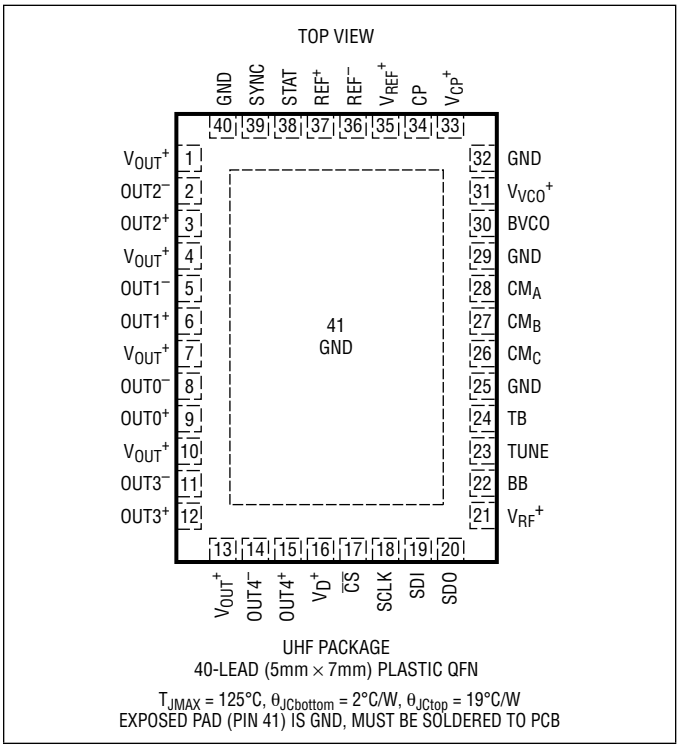
Operating Junction Temperature Range, T_J (Note 2)

LTC6951I and LTC6951I-1 ..... –40 to 105°C

Junction Temperature, T_{JMAX} ..... 125°C

Storage Temperature Range ..... –65 to 150°C

PIN CONFIGURATION



UHF PACKAGE
40-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 19°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC6951#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6951IUHF#PBF	LTC6951IUHF#TRPBF	6951	40-Lead (5mm × 7mm) Plastic QFN	–40°C to 105°C
LTC6951IUHF-1#PBF	LTC6951IUHF-1#TRPBF	69511	40-Lead (5mm × 7mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{OUT}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Inputs (REF^+, REF^-)							
f_{REF}	Input Frequency		●	1		425	MHz
V_{REF}	Input Signal Level	Single-Ended	●	0.5	2	2.7	V_{P-P}
	Minimum Input Slew Rate				20		V/µs
	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.65	1.85	2.25	V
	Input Signal Detected	REFOK = 1, PDREFPK = 0 10MHz ≤ f_{REF} ≤ 425MHz, Sine Wave	●	350			mV_{P-P}
	Input Signal Not Detected	REFOK = 0, PDREFPK = 0 10MHz ≤ f_{REF} ≤ 425MHz, Sine Wave	●			100	mV_{P-P}
	Input Resistance	Differential	●	2.6	4.2	6.1	kΩ
	Input Capacitance	Differential			7		pF
VCO							
f_{VCO}	Frequency Range	LTC6951 (Note 3) LTC6951-1 (Note 3)	● ●	4.0 4.3		5.0 5.4	GHz GHz
K_{VCO}	Tuning Sensitivity	(Notes 3, 4)			2.5 to 3.7		%Hz/V
Phase/Frequency Detector (PFD)							
f_{PFD}	Input Frequency		●			100	MHz
Charge Pump (CP)							
I_{CP}	Output Current Range	8 Settings (see Table 8)		1.0		11.2	mA
	Output Current Source/Sink Accuracy	All Settings, V(CP) = 2.3V				±6	%
	Output Current Source/Sink Matching	I_{CP} = 1.0mA to 1.4mA, V(CP) = 2.3V				±3.5	%
		I_{CP} = 2.0mA to 11.2mA, V(CP) = 2.3V				±2	%
	Output Current vs Output Voltage Sensitivity	(Note 5)	●		0.1	0.5	%/V
	Output Current vs Temperature	V(CP) = 2.3V	●		140		ppm/°C
	Output Hi-Z Leakage Current	I_{CP} = 1mA (Note 5)			0.5		nA
		I_{CP} = 11.2mA (Note 5)			5		nA
V_{MID}	Mid-Supply Output Bias Ratio	Referred to (V_{CP}^+ – GND)			0.48		V/V
Reference Divider (R)							
R	Divide Range	All Integers Included	●	1		63	Counts
VCO Divider (N)							
N	Divide Range	All Integers Included, RAO = 0	●	32		1023	Counts
		All Integers Included, RAO = 1	●	2		511	Counts
VCO Prescaler Divider (P)							
P	Divide Range	2, 2.5, 3, 3.5, 4 (see Table 14)	●	2		4	Counts
Digital Pin Specifications							
V_{IH}	High Level Input Voltage	$\overline{CS}$, SDI, SCLK, SYNC	●	1.55			V
V_{IL}	Low Level Input Voltage	$\overline{CS}$, SDI, SCLK, SYNC	●			0.8	V
V_{IHYS}	Input Voltage Hysteresis	$\overline{CS}$, SDI, SCLK, SYNC			250		mV
	Input Current	$\overline{CS}$, SDI, SCLK, SYNC	●			±1	µA
I_{OH}	High Level Output Current	SDO and STAT, $V_{OH} = V_D^+ - 400mV$	●		–3.3	–1.9	mA
I_{OL}	Low Level Output Current	SDO and STAT, V_{OL} = 400mV	●	2.0	3.4		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{OUT}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	SDO Hi-Z Current		●			±1	µA
Digital Timing Specifications (See Figure 13 and Figure 14)							
t_{CKH}	SCLK High Time		●	25			ns
t_{CKL}	SCLK Low Time		●	25			ns
t_{CSS}	$\overline{CS}$ Setup Time		●	10			ns
t_{CSH}	$\overline{CS}$ High Time		●	10			ns
t_{CS}	SDI to SCLK Setup Time		●	6			ns
t_{CH}	SDI to SCLK Hold Time		●	6			ns
t_{DO}	SCLK to SDO Time	to V_{IH}/V_{IL}/Hi-Z with 30pF Load	●			16	ns
SYNC Timing Specifications (See Figure 31 and Figure 32)							
t_{SYNCH}	SYNC High Time		●	1			ms
t_{SYNCL}	SYNC Low Time		●	1			ms
	SYNC Skew	EZSync, Part to Part				10	µs
t_{SS}	SYNC to REF Setup Time	(See Note 6)	●	1			ns
t_{SH}	SYNC to REF Hold Time	(See Note 6)	●	1			ns
Output Dividers (M0, M1, M2, M3 and M4)							
Mx	Output Divider Range (x = 0 to 4)	16 Settings (See Table 15)	●	1		512	Counts
Dx	Output Divider Delay (x = 0 to 4)	P Cycles, All Integers Included	●	0		255	Cycles
CML Clock Outputs (OUT0⁺, OUT0⁻, OUT1⁺, OUT1⁻, OUT2⁺, OUT2⁻, OUT3⁺, OUT3⁻), Differential Termination = 100Ω Unless Otherwise Noted							
f_{OUT}	LTC6951 Output Frequency		●	1.95		2500	MHz
		f_{OUT}/2 Subharmonic Generated, P = 2.5, Mx = 1 (Note 16)	●	1667		2000	MHz
		f_{OUT}/2 Subharmonic Generated, P = 3.5, Mx = 1 (Note 16)	●	1250		1333	MHz
	LTC6951-1 Output Frequency		●	2.1		2700	MHz
		f_{OUT}/2 Subharmonic Generated, P = 2.5, Mx = 1 (Note 16)	●	1800		2150	MHz
		f_{OUT}/2 Subharmonic Generated, P = 3.5, Mx = 1 (Note 16)	●	1350		1433	MHz
	Output High Voltage				$V_{OUT}^+ - 0.9$		V
	Output Low Voltage				$V_{OUT}^+ - 1.3$		V
	Output Differential Voltage		●	350	440	520	mV_{PK}
	Output Resistance	Differential, No Termination			100		Ω
t_R	Output Rise Time, 20% to 80%				50		ps
t_F	Output Fall Time, 80% to 20%				50		ps
	Output Duty Cycle	P = 2, 3, 4 all Mx, P = 2.5, 3.5 Mx ≥ 2 P = 2.5, Mx = 1 P = 3.5, Mx = 1	●	45	50 40 57	55	% % %
LVDS Clock Outputs (OUT4⁺, OUT4⁻), Differential Termination = 100Ω							
$f_{OUTLVDS}$	LTC6951 Output Frequency LTC6951-1 Output Frequency		● ●	1.95 2.1		800 800	MHz MHz
V_{OD}	Differential Output Voltage		●	300	380	450	mV_{PK}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{OUT}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\lvert\Delta V_{OD}\rvert$	Delta V_{OD}		●		5	50	mV
V_{OS}	Output Offset Voltage				1.23		V
$\lvert\Delta V_{OS}\rvert$	Delta V_{OS}		●		5	50	mV
t_{RLVDS}	Output Rise Time, 20% to 80%				200		ps
t_{FLVDS}	Output Fall Time, 80% to 20%				200		ps
	Short Circuit Current to Common	Shorted to GND	●		7.4	24	mA
	Short Circuit to Complementary				3.7		mA
	Output Duty Cycle	M4 ≥ 2	●	45	50	55	%
Clock Output Skews (OUT0⁺, OUT0⁻, OUT1⁺, OUT1⁻, OUT2⁺, OUT2⁻, OUT3⁺, OUT3⁻, OUT4⁺, OUT4⁻)							
t_{SKEW1}	Maximum Skew, from OUT0 to OUT1				±10	±35	ps
t_{SKEW2}	Maximum Skew, from OUT0 to OUT2				±10	±35	ps
t_{SKEW3}	Maximum Skew, from OUT0 to OUT3				±10	±35	ps
t_{SKEW4}	Maximum Skew, from OUT0 to OUT4				±20		ps
	Maximum Skew, All CML Outputs	One Part			±20	±40	ps
	Maximum Skew, All CML Outputs	Multiple Parts, RAO = SN = SR = 1			±50	±100	ps
Power Supply Voltages							
	V_{REF}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{OUT}^+ Supply Range		●	3.15	3.3	3.45	V
	V_D^+ Supply Range		●	3.15	3.3	3.45	V
	V_{RF}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{VCO}^+ Supply Range		●	4.75	5.0	5.25	V
	V_{CP}^+ Supply Range		●	4.2		5.25	V
Power Supply Currents							
I_{DDOUT}	V_D^+, V_{OUT}^+ Supply Current	Digital Inputs at Supply Levels, PDOUT=1			32		µA
		Digital Inputs at Supply Levels, SYNC = 3.3V	●		210	254	mA
I_{CC-5V}	Sum V_{CP}^+, V_{VCO}^+ Supply Currents	I_{CP} = 11.2mA	●		56	70	mA
		I_{CP} = 1.0mA	●		33	43	mA
		PDALL = 1			510		µA
$I_{CC-3.3V}$	Sum V_{REF}^+, V_{RF}^+ Supply Currents		●		115	130	mA
		PDALL = 1			140		µA
	V_D^+, V_{OUT}^+ Supply Current Deltas	MCx[1:0] = 2 (x = 0, 1, 2, or 3)			–31		mA
		MCx[1:0] = 3 (x = 0, 1, 2, or 3)			–43		mA
		MC4[1:0] = 2			–21		mA
		MC4[1:0] = 3			–34		mA
		SYNC = V_{OUT}^+ or SSYNC = 1			11		mA
Phase Noise and Spurious							
L_{VCO}	LTC6951 VCO Phase Noise (f_{VCO} = 4.0GHz, f_{OUT0} = 2.0GHz, P = 2, M0 = 1, Note 7)	10kHz Offset			–87		dBc/Hz
		100kHz Offset			–113		dBc/Hz
		1MHz Offset			–135		dBc/Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{OUT}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	LTC6951 VCO Phase Noise (f_{VCO} = 5.0GHz, f_{OUT0} = 2.5GHz, P = 2, M0 = 1, Note 7)	10kHz Offset			–83		dBc/Hz
		100kHz Offset			–110		dBc/Hz
		1MHz Offset			–133		dBc/Hz
	LTC6951-1 VCO Phase Noise (f_{VCO} = 5.4GHz, f_{OUT0} = 2.7GHz, P = 2, M0 = 1, Note 7)	10kHz Offset			–83		dBc/Hz
		100kHz Offset			–110		dBc/Hz
		1MHz Offset			–133		dBc/Hz
	LTC6951-1 CML Output Noise/Jitter (f_{VCO} = 5.4GHz, f_{OUT0} = f_{OUT1} = f_{OUT2} = f_{OUT3} = 2.7GHz, P = 2, M0 = M1 = M2 = M3 = 1, Notes 9, 12)	Phase Noise 10kHz Offset			–119		dBc/Hz
		Phase Noise 1MHz Offset			–129		dBc/Hz
		Phase Noise 40MHz Offset			–153		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			90		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			115		fs_{RMS}
	LTC6951 CML Output Noise/Jitter (f_{VCO} = 5.0GHz, f_{OUT0} = f_{OUT1} = f_{OUT2} = f_{OUT3} = 2.5GHz, P = 2, M0 = M1 = M2 = M3 = 1, Notes 9, 12)	Phase Noise 10kHz Offset			–119		dBc/Hz
		Phase Noise 1MHz Offset			–129		dBc/Hz
		Phase Noise 40MHz Offset			–153		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			90		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			115		fs_{RMS}
	LTC6951 CML Output Noise/Jitter (f_{VCO} = 5.0GHz, f_{OUT0} = f_{OUT1} = f_{OUT2} = f_{OUT3} = 1.25GHz, P = 2, M0 = M1 = M2 = M3 = 2, Notes 9, 12)	10kHz Offset			–125		dBc/Hz
		1MHz Offset			–135		dBc/Hz
		40MHz Offset			–156		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			88		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			115		fs_{RMS}
	LTC6951 CML Output Noise/Jitter (f_{VCO} = 4.0GHz, f_{OUT0} = f_{OUT1} = f_{OUT2} = f_{OUT3} = 250MHz, P = 4, M0 = M1 = M2 = M3 = 4, Notes 9, 12)	10kHz Offset			–140		dBc/Hz
		1MHz Offset			–150		dBc/Hz
		40MHz Offset			–165		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			83		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			115		fs_{RMS}
	LTC6951 LVDS Output Noise/Jitter (f_{VCO} = 4.0GHz, f_{OUT4} = 250MHz, P = 4, M4 = 4, Notes 9, 12)	10kHz Offset			–140		dBc/Hz
		1MHz Offset			–150		dBc/Hz
		40MHz Offset			–162		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			88		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			140		fs_{RMS}
L_{NORM}	Normalized In-Band Phase Noise Floor	I_{CP} = 11.2mA (Notes 8, 9, 10)			–229		dBc/Hz
$L_{1/f}$	Normalized In-Band 1/f Phase Noise	I_{CP} = 11.2mA (Notes 8, 11)			–277		dBc/Hz
	In-Band Phase Noise Floor	(Notes 8, 9, 10, 13)			–134		dBc/Hz
	Integrated Phase Noise from 100Hz to 40MHz	(Notes 9, 13)			0.015		°RMS
	Spurious	f_{OFFSET} = f_{PFD}, PLL Locked (Notes 9, 13, 14, 15)			–95		dBc

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6951IUHF and LTC6951IUHF-1 are guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 105°C. Under maximum operating conditions, air flow or heat sinking may be required to maintain a junction temperature of 105°C or lower. It is strongly recommended that the Exposed Pad (Pin 41) be soldered directly to the ground plane with an array of thermal vias as described in the Applications Information section.

Note 3: Valid for 1.50V ≤ V(TUNE) ≤ 2.85V with part calibrated after a power cycle or software power-on-reset (POR).

Note 4: Based on characterization.

Note 5: For 1.4V < V(CP) < 3.0V.

Note 6: Measurement requires RAO = 1 with SR = 1 at SYNC rising edge and SN = 1 at SYNC falling edge. REF^+ is a CMOS level signal with a 1ns rise time and the measurement point at the 50% crossing. SYNC is a CMOS level signal with a 1ns rise and fall time. For SYNC rising and SR = 1, the measurement point is 1.55V. For SYNC falling and SN = 1, the measurement point is 0.8V.

Note 7: Measured outside the loop bandwidth, using a narrowband loop.

Note 8: Measured inside the loop bandwidth with the loop locked.

Note 9: Reference frequency supplied by Wenzel 501-04516, f_{REF} = 100MHz, P_{REF} = 10dBm.

Note 10: Output Phase Noise Floor is calculated from Normalized Phase Noise Floor by $L_{OUT} = L_{NORM} + 10\log_{10}(f_{PFD}) + 20\log_{10}(f_{OUTx}/f_{PFD})$.

Note 11: Output 1/f Noise is calculated from Normalized 1/f Phase Noise by $L_{OUT(1/f)} = L_{1/f} + 20\log_{10}(f_{OUTx}) – 10\log_{10}(f_{OFFSET})$.

Note 12: I_{CP} = 11.2mA, f_{PFD} = 100MHz, FILT = 0, Loop BW = 340kHz

Note 13: I_{CP} = 11.2mA, f_{PFD} = 100MHz, FILT = 0, Loop BW = 340kHz; f_{OUT0} = 500MHz, f_{VCO} = 4.0GHz.

Note 14: Measured using DC2248A.

Note 15: Measured using differential LTC6951 outputs driving LTC6954. LTC6954 provides differential to single-ended conversion for rejection of common mode spurious signals. See the Applications Information section for details.

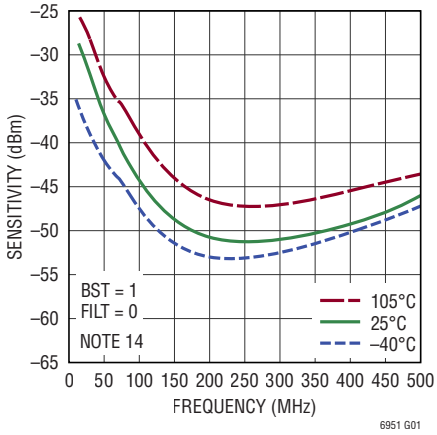
Note 16: When P = 2.5 or 3.5 and Mx = 1, a subharmonic of approximately –45dBc to –25dBc is generated at the output at $f_{OUT}/2$. While most applications are not affected by this spur, some, such as ADC and DAC sampling, are degraded. For applications sensitive to subharmonic spurs, these settings are not recommended unless the output frequency is further divided by at least 2 (i.e. ADC clock divider).

Note 17: Each output can be individually powered down by setting the output's MCx[1:0] bits to 3. See Tables 16 and 17.

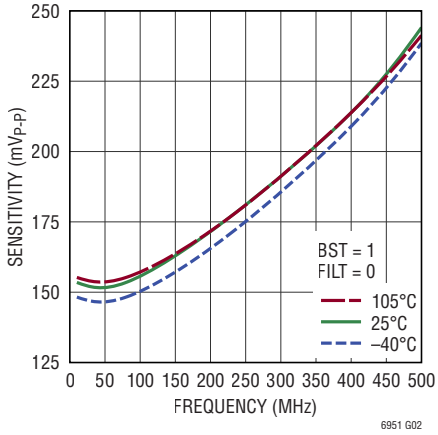
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_{OUT}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, Unless otherwise noted.

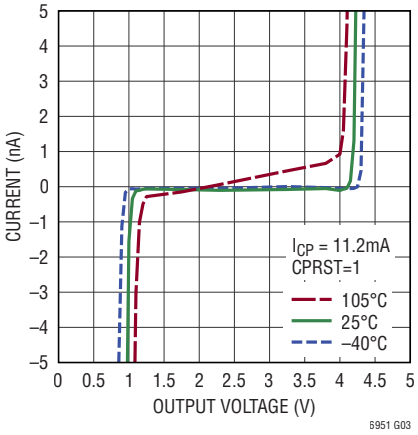
REF Input Sensitivity vs Frequency



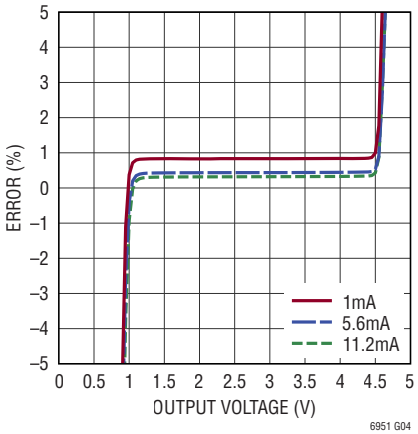
REF Input Signal Detected vs Frequency, Temperature



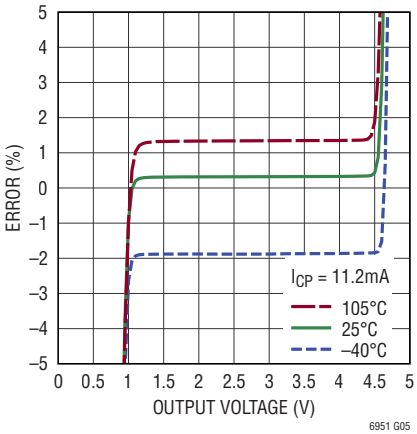
Charge Pump Hi-Z Current vs Voltage, Temperature



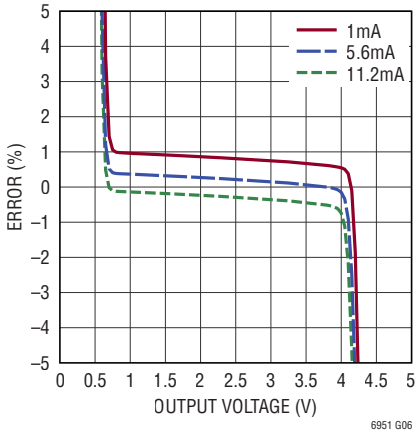
Charge Pump Sink Current Error vs Voltage, Output Current



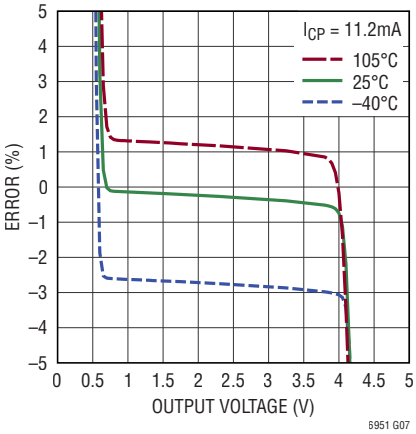
Charge Pump Sink Current Error vs Temperature



Charge Pump Source Current Error vs Voltage, Output Current



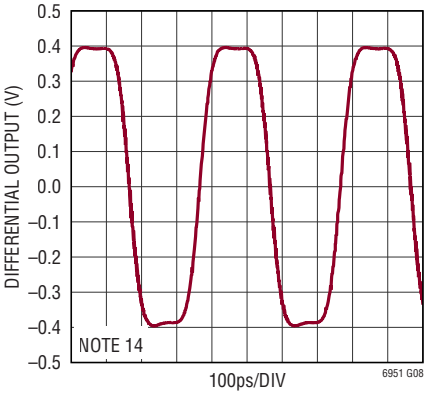
Charge Pump Source Current Error vs Voltage, Temperature



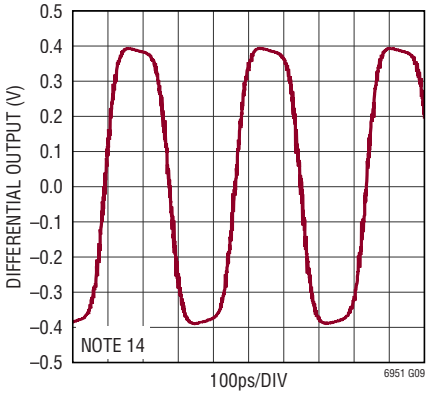
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_{OUT}^+ = V_D^+ = V_{RF}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$, Unless otherwise noted.

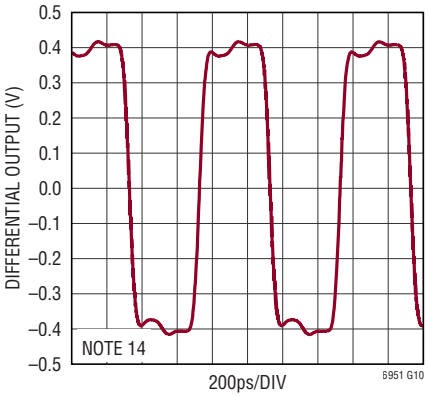
LTC6951 CML Differential Output at 2.5GHz



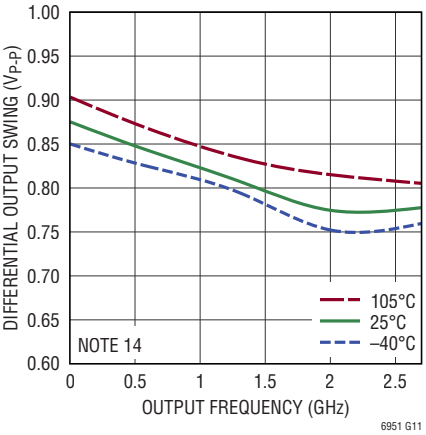
LTC6951-1 CML Differential Output at 2.7GHz



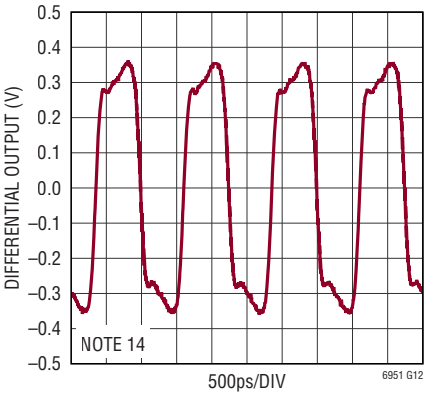
LTC6951 CML Differential Output at 1.25GHz



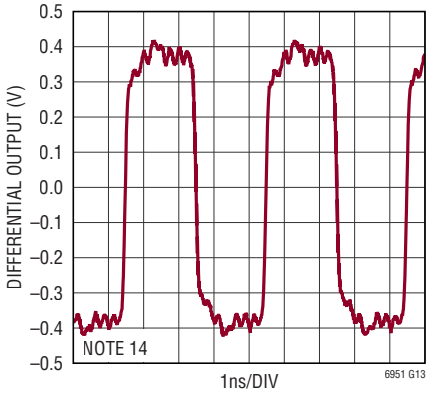
CML Differential Output Swing vs Frequency, Temperature



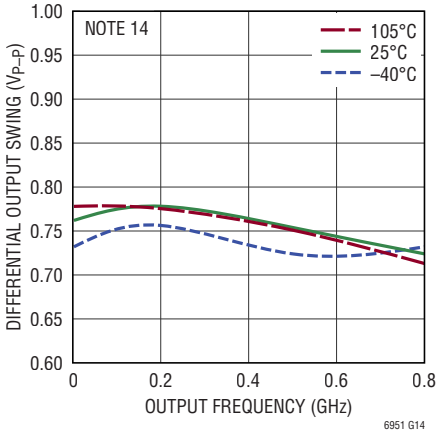
LVDS Differential Output at 800MHz



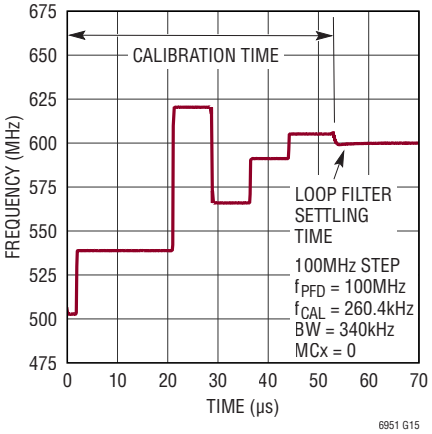
LVDS Differential Output at 250MHz



LVDS Differential Output Swing vs Frequency, Temperature



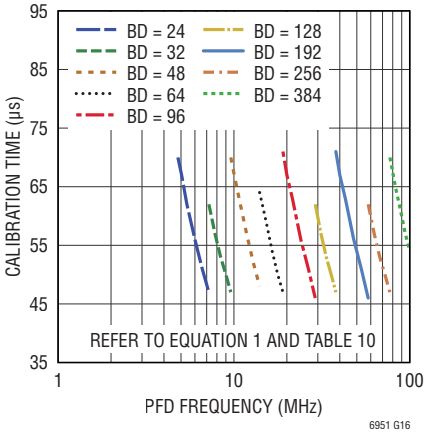
Frequency Step Transient, RAO = 0



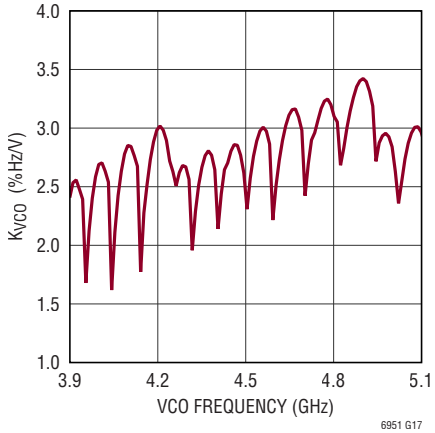
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_{OUT}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, Unless otherwise noted.

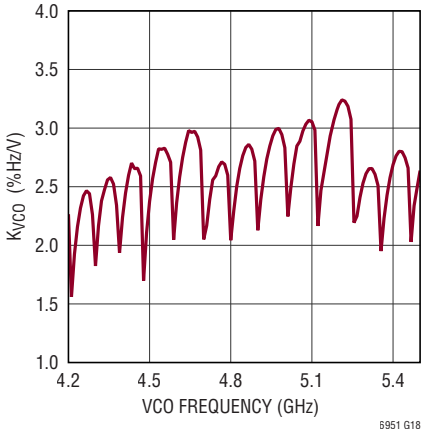
Max Calibration Time (RAO = 0) vs f_{PD}, B Divide Value



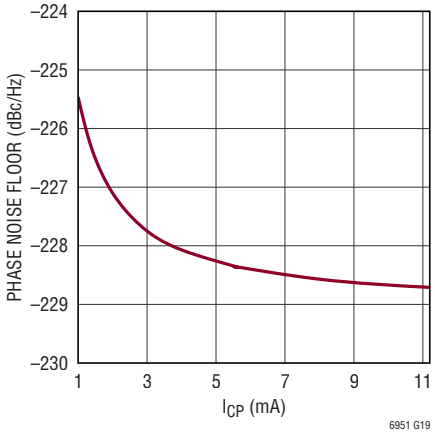
LTC6951 VCO Tuning Sensitivity



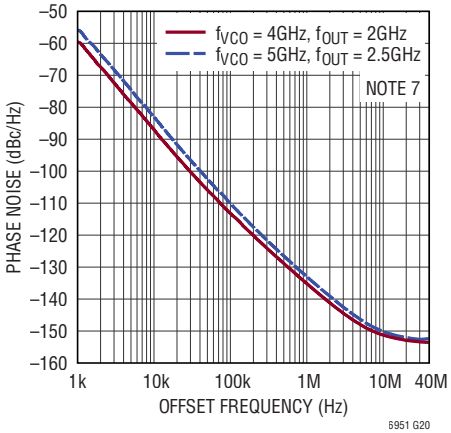
LTC6951–1 VCO Tuning Sensitivity



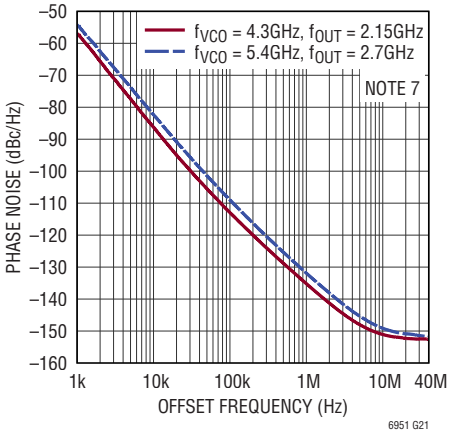
Normalized In-Band Phase Noise Floor vs CP Current



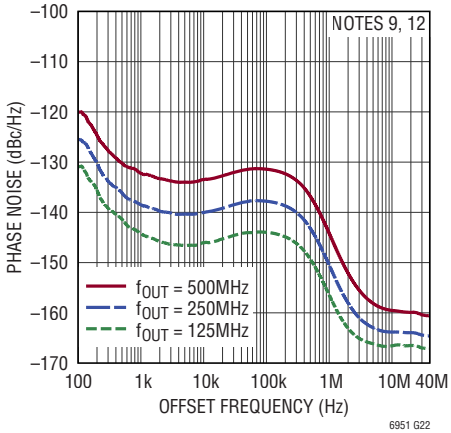
LTC6951 VCO Phase Noise at CML Outputs, P = 2, Mx = 1



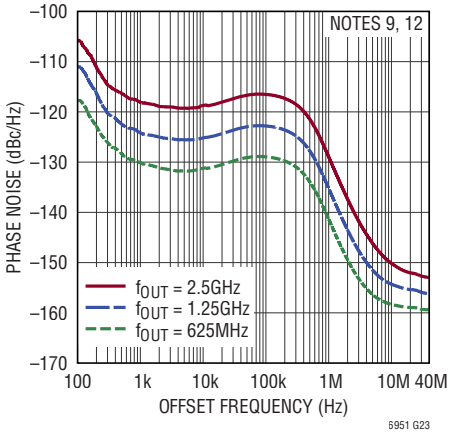
LTC6951-1 VCO Phase Noise at CML Outputs, P = 2, Mx = 1



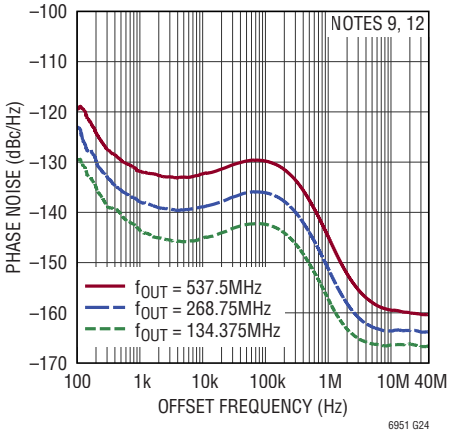
LTC6951 Phase Noise at CML Outputs, f_{VCO} = 4GHz, P = 2, Mx = 4, 8 and 16



LTC6951 Phase Noise at CML Outputs, f_{VCO} = 5GHz, P = 2, Mx = 1, 2 and 4



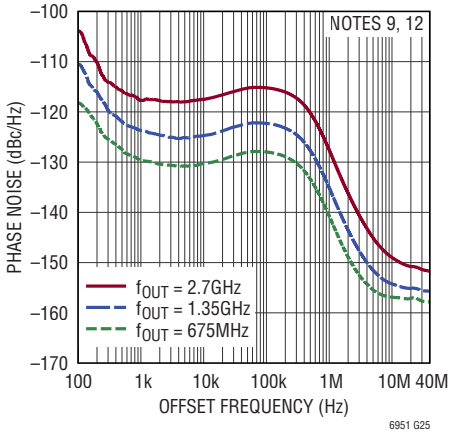
LTC6951-1 Phase Noise at CML Outputs, f_{VCO} = 4.3GHz, P = 2, Mx = 4, 8 and 16



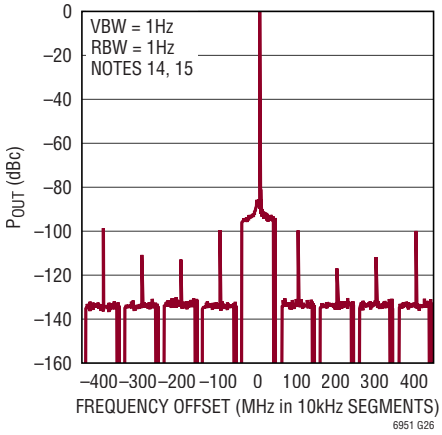
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_{OUT}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, Unless otherwise noted.

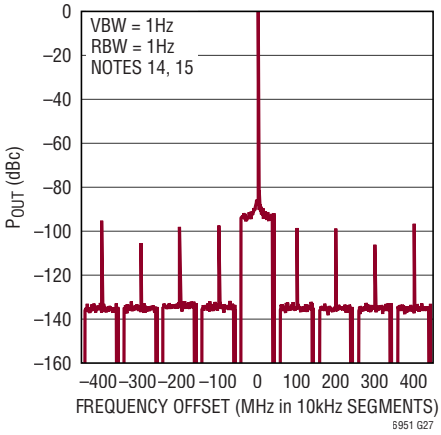
LTC6951-1 Phase Noise at CML Outputs, f_{VCO} = 5.4GHz, P = 2, Mx = 1, 2 and 4



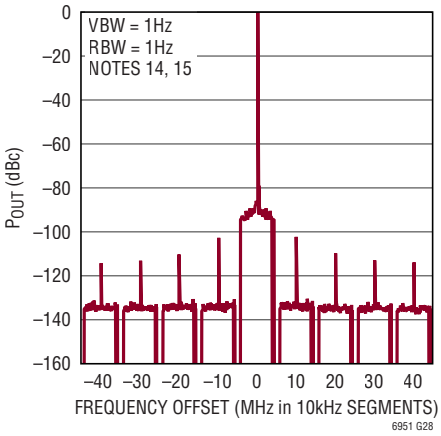
Spurious Response f_{RF} = 1250MHz, f_{REF} = 100MHz, f_{PFD} = 100MHz, Loop BW = 340kHz



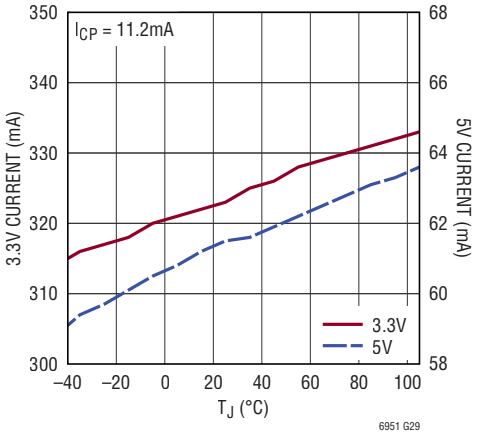
Spurious Response f_{RF} = 500MHz, f_{REF} = 100MHz, f_{PFD} = 100MHz, Loop BW = 340kHz



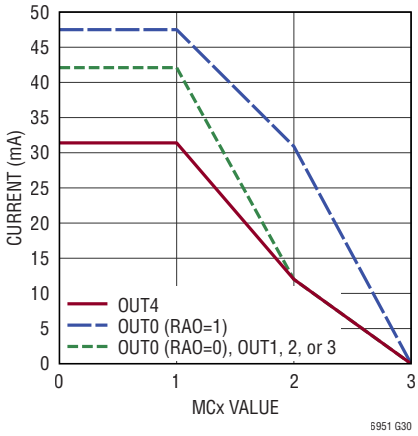
Spurious Response f_{RF} = 500MHz, f_{REF} = 100MHz, f_{PFD} = 10MHz, Loop BW = 290kHz



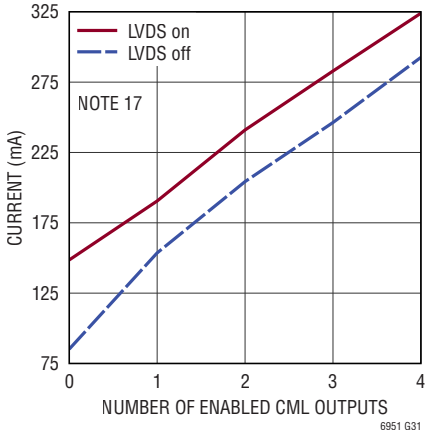
Supply Current vs Temperature RAO = 0, All Outputs Enabled



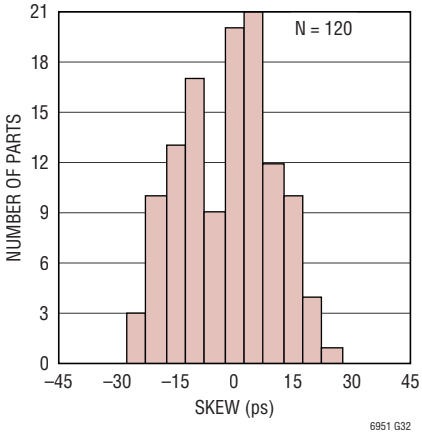
V_{OUT}^+ Supply Current per Output vs MCx Value



3.3V Supply Current vs Number of Enabled CML Outputs



Part to Part Skew,CML Outputs, f_{OUT} = 1GHz



PIN FUNCTIONS

V_{OUT}^+, V_D^+ (Pins 1, 4, 7, 10, 13, 16): 3.15V to 3.45V Positive Supply Pins for Output Dividers, SYNC Function and Serial Port. Each pin should be separately bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible. V_{OUT}^+, V_D^+, V_{RF}^+, and V_{REF}^+ must all be at the same voltage.

OUT2⁻, OUT2⁺ (Pins 2, 3): 2.5V CML Output Signals. The M2 output divider is buffered and presented differentially on these pins. The outputs are connected with 50Ω (typical) pull-up resistors tied to an internal resistive common mode point. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

OUT1⁻, OUT1⁺ (Pins 5, 6): 2.5V CML Output Signals. The M1 output divider is buffered and presented differentially on these pins. The outputs are connected with 50Ω (typical) pull-up resistors tied to an internal resistive common mode point. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

OUT0⁻, OUT0⁺ (Pins 8, 9): 2.5V CML Output Signals. The M0 output divider is buffered and presented differentially on these pins. The outputs are connected with 50Ω (typical) pull-up resistors tied to an internal resistive common mode point. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

OUT3⁻, OUT3⁺ (Pins 11, 12): 2.5V CML Output Signals. The M3 output divider is buffered and presented differentially on these pins. The outputs are connected with 50Ω (typical) pull-up resistors tied to an internal resistive common mode point. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

OUT4⁻, OUT4⁺ (Pins 14, 15): LVDS Output Signals. The M4 output divider is buffered and presented differentially on these pins. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

$\overline{CS}$ (Pin 17): Serial Port Chip Select. This CMOS input initiates a serial port communication burst when driven low, ending the burst when driven back high. See the Operation section for more details.

SCLK (Pin 18): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. See the Operation section for more details.

SDI (Pin 19): Serial Port Data Input. The serial port uses this CMOS input for data. See the Operation section for more details.

SDO (Pin 20): Serial Port Data Output. This CMOS three-state output presents data from the serial port during a read communication burst. Optionally attach a resistor of > 200kΩ to GND to prevent a floating output. See the Applications Information section for more details.

V_{RF}^+ (Pin 21): 3.15V to 3.45V Positive Supply Pin for RF Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible. V_{OUT}^+, V_D^+, V_{RF}^+, and V_{REF}^+ must all be at the same voltage.

BB (Pin 22): RF Reference Bypass. This output has a 6.5k resistance and must be bypassed with a 0.47µF ceramic capacitor to GND. Do not couple this pin to any other signal.

TUNE (Pin 23): VCO Tuning Input. This frequency control pin is normally connected to the external loop filter. See the Applications Information section for more details.

TB (Pin 24): VCO Bypass. This output has a 7k resistance and must be bypassed with a 1.0µF ceramic capacitor to GND. It is normally connected to CM_A, CM_B, and CM_C with a short trace. Do not couple this pin to any other signal.

PIN FUNCTIONS

GND (Pins 25, 29, Exposed Pad Pin 41): Negative Power Supply (Ground). These pins should be tied directly to the ground plane with multiple vias for each pin. The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance.

CM_C, CM_B, CM_A (Pins 26, 27, 28): VCO Bias Inputs. These inputs are normally connected to TB with a short trace and bypassed with a 1µF ceramic capacitor to GND. Do not couple these pins to any other signal. *For best phase noise performance, DO NOT place a trace between these pads underneath the package.*

BVCO (Pin 30): VCO Bypass Pin. This output must be bypassed with a 1.0µF ceramic capacitor to GND. Do not couple this pin to any other signal.

V_{VCO}^+ (Pin 31): 4.75V to 5.25V Positive Supply Pin for VCO Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

GND (Pins 32, 40): Negative Power Supply (Ground). These pins are attached directly to the Die Attach Paddle (DAP) and should be tied directly to the ground plane.

V_{CP}^+ (Pin 33): 4.2V to 5.25V Positive Supply Pin for Charge Pump Circuitry. This pin should be bypassed directly to the ground plane using two ceramic capacitors of 1µF and 0.01µF as close to the pin as possible. Additionally, a 10Ω resistor should be added in series with the 5V power supply to reduce switching noise. The resistor should be placed between the 5V supply rail and the two ceramic capacitors.

CP (Pin 34): Charge Pump Output. This bidirectional current output is normally connected to the external loop filter. See the Applications Information section for more details.

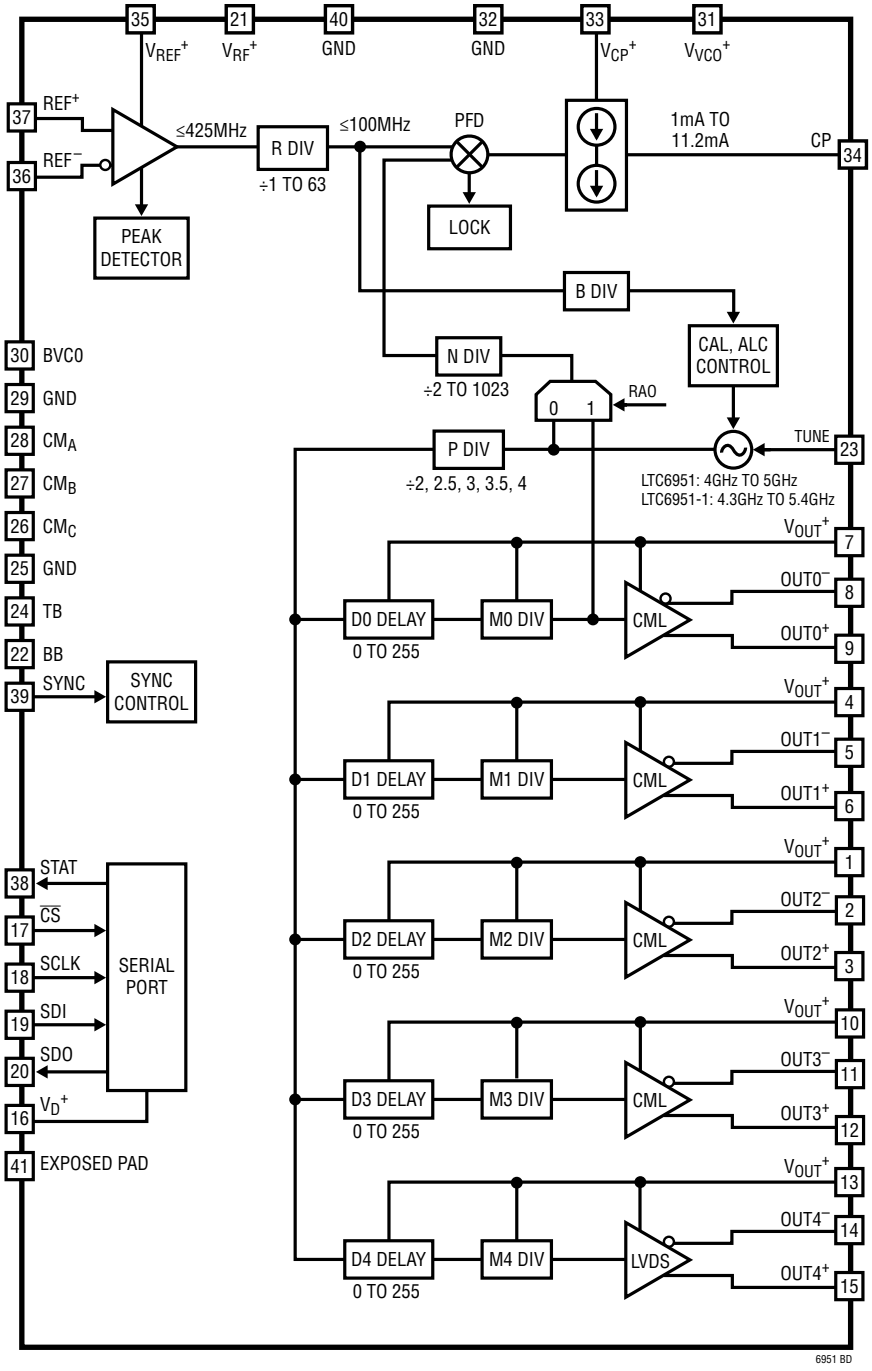
V_{REF}^+ (Pin 35): 3.15V to 3.45V Positive Supply Pin for Reference Input Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible. V_{OUT}^+, V_D^+, V_{RF}^+, and V_{REF}^+ must all be at the same voltage.

REF^-, REF^+ (Pins 36, 37): Reference Input Signals. This differential input is buffered with a low noise amplifier, which feeds the reference divider. They are self-biased and must be AC-coupled with 1µF capacitors. If used single-ended with $V(REF^+) \leq 2.7V_{P-P}$, bypass REF^- to GND with a 1µF capacitor. If used single-ended with $V(REF^+) > 2.7V_{P-P}$, bypass REF^- to GND with a 47pF capacitor.

STAT (Pin 38): Status Output. This signal is a configurable logical OR combination of the UNLOCK, ALCHI, ALCLO, $\overline{LOCK}$, LOCK, $\overline{REFOK}$, and REFOK status bits, programmable via the STATUS register. See the Operation section for more details.

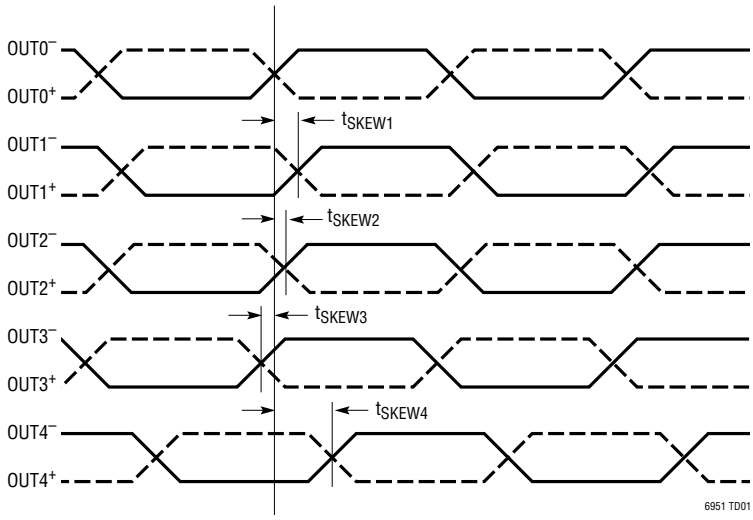
SYNC (Pin 39): Synchronization Input. This CMOS input stops the output dividers when driven high and initiates synchronization when driven back low when enabled for each output. When using the SSYNC software synchronization bit, the SYNC pin must be held at a logic low state. See the Operation and Applications Information section for more details.

BLOCK DIAGRAM

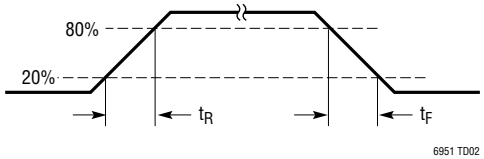


TIMING DIAGRAMS

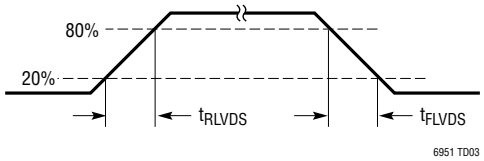
Output Skews



Differential CML Rise/Fall Times



Differential LVDS Rise/Fall Times



OPERATION

The LTC6951 is a high-performance integer-N PLL, complete with a low noise VCO. Its multi-output clock generator incorporates Linear Technology's proprietary EZSync and ParallelSync standards, allowing synchronization across multiple outputs and multiple chips. The device is able to achieve superior integrated jitter performance by the combination of its extremely low in-band phase noise and excellent VCO noise characteristics.

REFERENCE INPUT BUFFER

The PLL's reference frequency is applied differentially on pins REF⁺ and REF⁻. These high-impedance inputs are self-biased and must be AC-coupled with 1µF capacitors (see Figure 1 for a simplified schematic). Alternatively, the inputs may be used single-ended by applying the reference frequency at REF⁺ and bypassing REF⁻ to GND with a 1µF capacitor. If the single-ended signal is greater than $2.7V_{P-P}$, then use a 47pF capacitor for the GND bypass.

A high quality signal must be applied to the REF± inputs as they provide the frequency reference to the entire PLL. To achieve the part's in-band phase noise performance, apply a sine wave signal of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 20V/µs. Figure 2 shows recommended interfaces for different reference types.

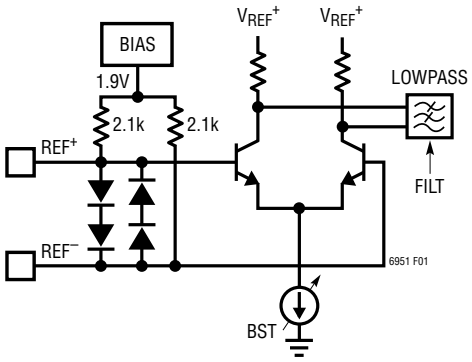


Figure 1. Simplified REF Interface Schematic

Additional options are available through serial port register h03 to further refine the application. Bit FILT controls the reference input buffer's low-pass filter, and should be set for sine wave signals based upon f_{REF} to limit the reference's wideband noise. The FILT bit must be set correctly to reach the L_{NORM} normalized in-band phase noise floor. See Table 1 for recommended settings. Square wave inputs will have FILT set to "0".

OPERATION

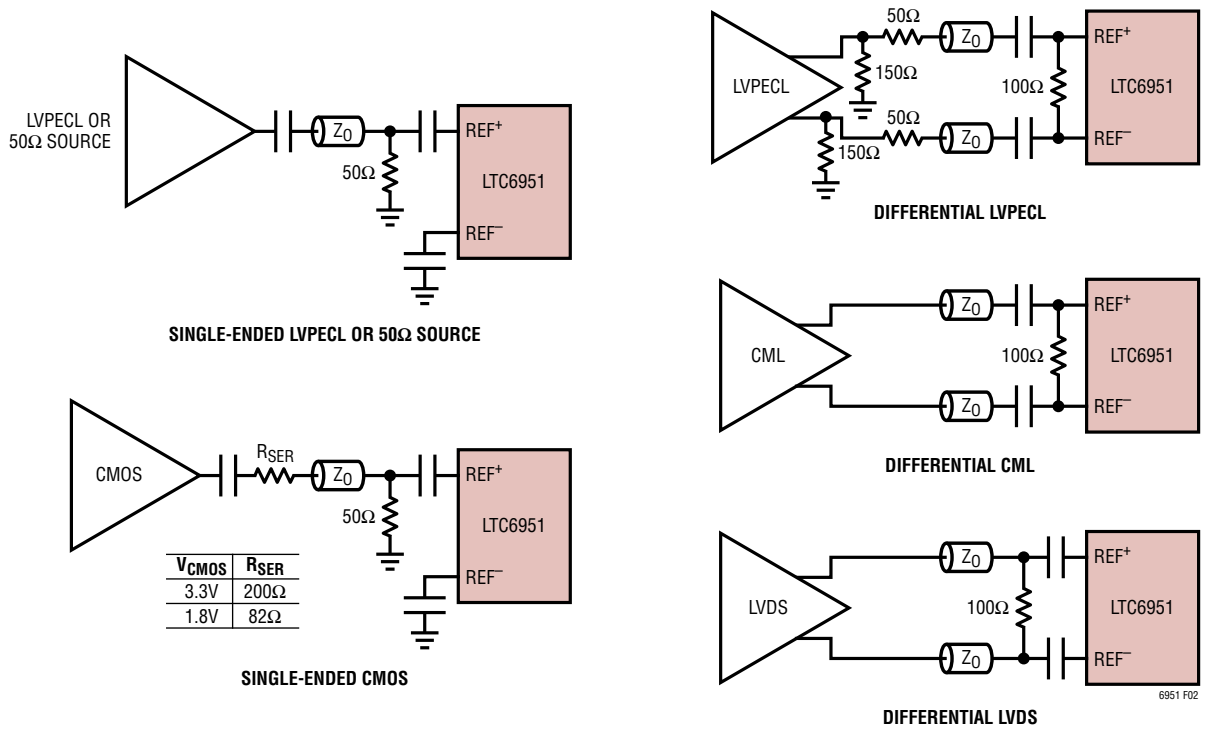


Figure 2. Common Reference Input Interface Configurations. All Z_0 Signal Traces Are 50Ω Transmission Lines and All Caps Are 1µF

Table 1. FILT Programming

FILT	Sine Wave f_{REF}	Square Wave f_{REF}
1	<20MHz	N/A
0	≥20MHz	All f_{REF}

The BST bit should be set based upon the input signal level to prevent the reference input buffer from saturating. The BST programming is the same whether the input is a sine wave or a square wave. See Table 2 for recommended settings and the Applications Information section for programming examples.

Table 2. BST Programming

BST	V_{REF}
1	<1.6V_{P-P}
0	≥1.6V_{P-P}

Peak Detector

A reference input peak detection circuit is provided on the REF± inputs to detect the presence of a reference signal and provides the REFOK and $\overline{\text{REFOK}}$ status flags available through both the STAT output and serial port register h00. $\overline{\text{REFOK}}$ is the logical inverse of REFOK. The circuit has hysteresis to prevent the REFOK flag from chattering at the detection threshold. The reference peak detector may be powered-down using the PDREFPK bit found in register h02.

The peak detector approximates an RMS detector, therefore sine and square wave inputs will give different detection thresholds by a factor of 4/π. See Table 3 for REFOK detection values.

Table 3. REFOK, $\overline{\text{REFOK}}$ Status Output vs REF Input

REFOK	$\overline{\text{REFOK}}$	Sine Wave f_{REF}	Square Wave f_{REF}
1	0	≥350mV_{P-P}	≥275mV_{P-P}
0	1	<100mV_{P-P}	<75mV_{P-P}

OPERATION

REFERENCE ALIGNED OUTPUT (RAO)

The RAO bit (register h03) controls the fundamental configuration of the PLL. Figure 3 shows the PLL loop diagram with bit RAO set to "0", which is the power-up default. All five outputs can be synchronized and delayed relative to each other, but will not be aligned to the Reference input. Systems needing alignment to the Reference input either on an individual basis or across multiple LTC6951s can set RAO to "1" to have the PLL loop diagram as shown in Figure 4. The P and M0 dividers are now part of the overall feedback loop. Table 4 describes the differences in the PLL feedback elements versus the RAO bit setting. Only when the P and M0 dividers are in the feedback loop can the output rising edges be coincident with the N divider output and by inference the R divider output.

When RAO is set to a "1", bits SR and SN become active and allow known and repeatable latency to the outputs in addition to known alignment to the Reference input. Figure 5 shows the operation of the SR bit and Figure 11 shows the operation of the SN bit. Table 5 is a brief description of the SR and SN functions. See the ParallelSync Multi-Chip Synchronization Example in the Applications Information section for a programming example and output timing diagrams of the RAO mode.

Table 4. RAO Programming

RAO	PLL FEEDBACK ELEMENTS
0	N Divider
1	N, P, M0 Dividers

Table 5. SN and SR Function Description

RAO	SN	SR	Description
0	NA	NA	Unknown phase relationship from REF input to outputs, EZSync timing.
1	0	0	Outputs phase aligned to REF input, unknown SYNC to output latency, EZSync timing.
1	1	1	Outputs phase aligned to REF input, known SYNC to output latency, critical SYNC to REF timing.

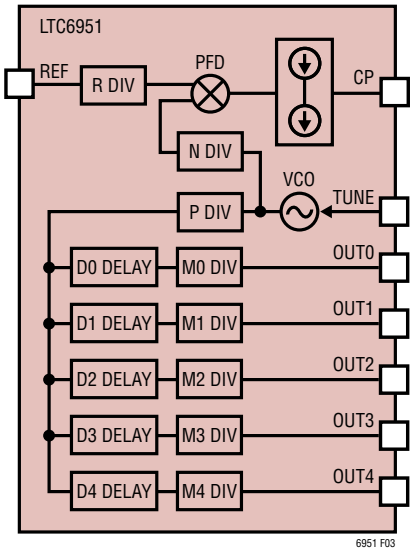


Figure 3. PLL loop diagram, RAO = 0

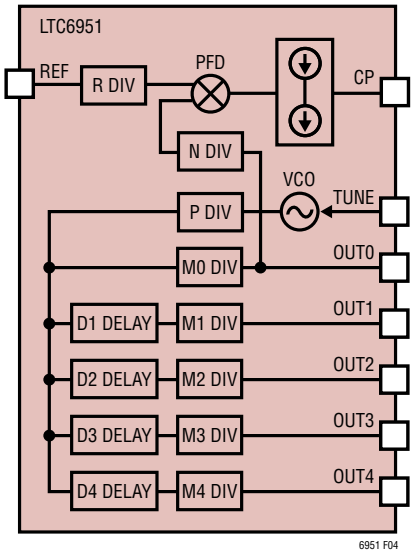


Figure 4. PLL loop diagram, RAO = 1

OPERATION

REFERENCE DIVIDER (R)

A 6-bit divider is used to reduce the frequency seen at the PFD. Its divide ratio R may be set to any integer from 1 to 63. Use the RD[5:0] bits found in register h05 to directly program the R divide ratio. See the Applications Information section for the relationship between R and the f_{REF}, f_{PFD}, f_{VCO} and f_{OUTx} frequencies.

A mode to provide synchronization of the Reference inputs to the R divider output (R ≥ 2) using the SYNC pin input rising edge is enabled when bits RAO in register h03 and SR in register h0A are set to "1". The SYNC pin rising edge must meet setup and hold timing to the rising edge of the Reference input. See Figure 5 for the timing relationships between the Reference input, SYNC and the R divider output. Note that changing the R divider output edge timing will force the PLL to lose phase lock but will return to normal operation after several loop time constants. See Reference Signal and Sync Timing for SR and SN Modes in the Applications Information section for the timing requirements of SYNC to REF in this mode.

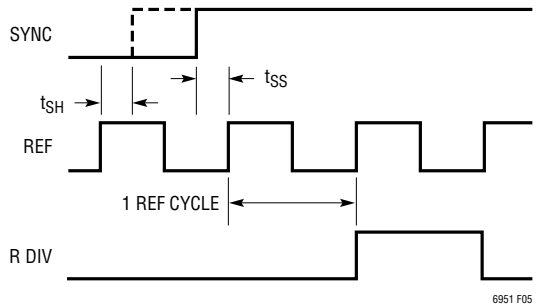


Figure 5. SYNC to REF timing (RAO = SR = 1)

PHASE/FREQUENCY DETECTOR (PFD)

The phase/frequency detector (PFD), in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the R and N dividers. This action provides the necessary feedback to phase-lock the loop, forcing a phase alignment at the PFD's inputs. The PFD may be disabled with the CPRST bit which prevents UP and DOWN pulses from being produced. See Figure 6 for a simplified schematic of the PFD.

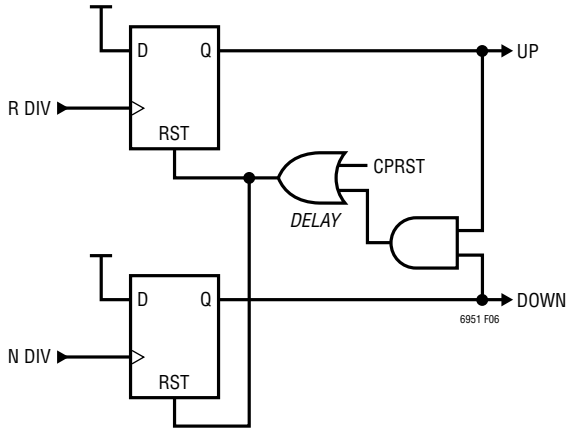


Figure 6. Simplified PFD Schematic

LOCK INDICATOR

The lock indicator uses internal signals from the PFD to measure phase coincidence between the R and N divider output signals. It is enabled by programming LKCT[1:0] in the serial port register h04 (see Table 7), and produces LOCK, $\overline{\text{LOCK}}$ and UNLOCK status flags, available through both the STAT output and serial port register h00. $\overline{\text{LOCK}}$ is the logical inverse of LOCK.

Note that f_{REF} must be present for the LOCK and UNLOCK flags to properly assert and clear.

The user sets the phase difference lock window time t_{LWW} for a valid LOCK condition with the LKWIN bit found in register h04. Table 6 contains recommended settings for different f_{PFD} frequencies. See the Applications Information section for examples.

Table 6. LKWIN Programming

LKWIN	t_{LWW}	f_{PFD}
0	5.0ns	>4.7MHz
1	10.7ns	≤4.7MHz

OPERATION

The PFD phase difference must be less than t_{LWW} for the COUNTS number of successive counts before the lock indicator asserts the LOCK flag. The LKCT[1:0] bits are used to set COUNTS depending upon the application. Set LKCT[1:0] = 0 to disable the lock indicator. See Table 7 for LKCT[1:0] programming and the Applications Information section for examples.

Table 7. LKCT[1:0] Programming

LKCT[1:0]	COUNTS
0	Lock Indicator Disabled
1	32
2	256
3	2048

When the PFD phase difference is greater than t_{LWW}, the lock indicator immediately asserts the UNLOCK status flag and clears the LOCK flag, indicating an out-of-lock condition. The UNLOCK flag is immediately de-asserted when the phase difference is less than t_{LWW}. See Figure 7 below for more details.

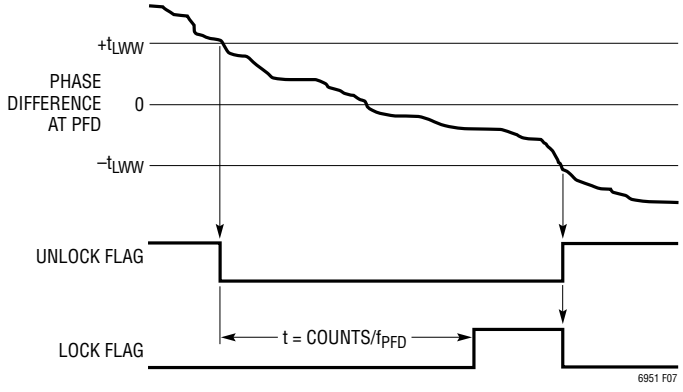


Figure 7. UNLOCK and LOCK Timing

CHARGE PUMP (CP)

The charge pump, controlled by the PFD, forces sink (DOWN) or source (UP) current pulses onto the CP pin, which should be connected to an appropriate loop filter. See Figure 8 for a simplified schematic of the charge pump.

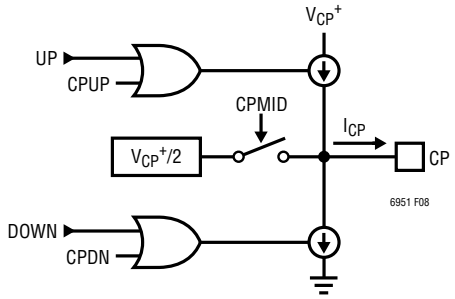


Figure 8. Simplified Charge Pump Schematic

The output current magnitude I_{CP} may be set from 1mA to 11.2mA using the CP[2:0] bits found in serial port register h07. A larger I_{CP} can result in lower in-band noise due to the lower impedance of the loop filter components. See Table 8 for programming specifics and the Applications Information section for loop filter examples.

Table 8. CP[2:0] Programming

CP[2:0]	I_{CP}
0	1.0mA
1	1.4mA
2	2.0mA
3	2.8mA
4	4.0mA
5	5.6mA
6	8.0mA
7	11.2mA

OPERATION

Charge Pump Functions

The charge pump contains additional features to aid in system startup. See Table 9 below for a summary.

Table 9. Charge Pump Function Bit Descriptions

BIT	DESCRIPTION
CPDN	Force sink current.
CPMID	Enable mid-voltage bias.
CPRST	Reset PFD, Hi-Z CP.
CPUP	Force source current.
CPWIDE	Extend current pulse width.

The CPMID bit found in register h07 enables a resistive V_{CP}+/2 output bias which may be used to pre-bias troublesome loop filters into a valid voltage range. When using CPMID, it is recommended to also assert the CPRST bit, forcing a PFD reset which puts the charge pump into a Hi-Z state. Both CPMID and CPRST must be set to "0" for normal operation.

The CPUP and CPDN bits force a constant I_{CP} source or sink current, respectively, on the CP pin. The CPRST bit may also be used in conjunction with the CPUP and CPDN bits, allowing a pre-charge of the loop to a known state, if required. CPUP, CPDN, and CPRST must be set to "0" to allow the loop to lock.

The CPWIDE bit extends the charge pump output current pulse width by increasing the PFD reset path's delay value. CPWIDE is normally set to "0". Setting CPWIDE = 0 provides the best in-band phase noise performance.

VCO

The integrated VCO operates from 4GHz to 5GHz for the LTC6951 and 4.3GHz to 5.4GHz for the LTC6951-1. The frequency range of the VCO, coupled with the output prescaler and output divider capability, allows the LTC6951 to cover an extremely wide range of continuously selectable frequencies.

The BB and TB pins are used to bias internal VCO circuitry. The BB pin has a 6.5kΩ output resistance and should be bypassed with a 0.47µF ceramic capacitor to GND, giving a time constant of 3ms. The TB pin has a 7kΩ output resistance and should be bypassed with a 1µF ceramic capacitor to GND, resulting in a time constant of 7ms. Stable bias voltages are achieved after approximately three time constants following power-up or after deasserting the PDPLL or PDVCO bits.

VCO Calibration

The VCO must be calibrated each time its frequency is modified by any change in f_{REF}, the R divider value, or the N divider value when RAO = 0. Additionally when RAO = 1, any change in f_{REF}, the R divider value, the N divider value, the P divider value, or the M0 divider value requires VCO calibration (see the Applications Information section for the relationship between R, N, P, Mx, and the f_{REF}, f_{PFD}, f_{VCO}, and f_{OUTx} frequencies). *The output frequency is then stable over the LTC6951's entire temperature range, regardless of the temperature at which it was calibrated, until the part is reset due to a power cycle or software power-on-reset (POR).*

The output of the B divider is used to clock digital calibration circuitry as shown in the Block Diagram. The B value, programmed with bits BD[3:0], is dependent on the setting of the RAO bit. The relationship between bits BD[3:0], the B value, and f_{PFD} for RAO = 0 is shown in Table 10.

Table 10. BD[3:0] Programming, RAO = 0

BD[3:0]	B DIVIDE VALUE	f_{PFD} (MHz)
0	8	<2.4
1	12	2.4 to 3.6
2	16	3.6 to 4.8
3	24	4.8 to 7.2
4	32	7.2 to 9.6
5	48	9.6 to 14
6	64	14 to 19
7	96	19 to 29
8	128	29 to 38
9	192	38 to 58
10	256	58 to 77
11	384	>77
12 to 15	Invalid	

OPERATION

The relationship between bits BD[3:0], the B value, and the N value for RAO = 1 is shown in Table 11.

Table 11. BD[3:0] Programming, RAO = 1

BD[3:0]	B DIVIDE VALUE	N DIVIDE VALUE
0	8	NA
1	12	240 to 511
2	16	180 to 239
3	24	120 to 179
4	32	90 to 119
5	48	60 to 89
6	64	45 to 59
7	96	30 to 44
8	128	23 to 29
9	192	12 to 22
10	256	4 to 11
11	384	2 to 3
12 to 15	Invalid	

Once the RD[5:0], ND[9:0], and BD[3:0] bits are written and the reference frequency f_{REF} is present and stable at the REF± inputs, the VCO must be calibrated by setting CAL = 1 (the bit self-clears when calibration is complete). The calibration cycle takes between 12 and 14 clocks of the B divider output with the nominal calibration time shown in Equation 1. Setting bits MCx[1:0] = 1 selectively mutes the outputs during the calibration.

$$t_{CAL} = \frac{14 \bullet B}{f_{PFD}} \quad (1)$$

Note that the f_{REF} frequency and TB and BB voltages must be stable for proper calibration. Stable bias voltages are achieved after approximately three time constants (about 25ms) following power-up.

Setting AUTOCAL = 1 causes the CAL bit to be set automatically whenever serial port registers h05 or h06 are written. When AUTOCAL is enabled and RAO = 0, there is no need for a separate register write to set the CAL bit.

When RAO =1 the loop also uses the P and M0 divide values which are located in registers h08 and h09 which when changed will not trigger the CAL bit with AUTOCAL = 1.

It is recommended to set AUTOCAL = 0 in this mode and to calibrate the VCO by setting CAL = 1 after all the appropriate registers have been written. See Table 12 for a summary of the VCO bits.

Table 12. VCO Bit Descriptions

BIT	DESCRIPTION
AUTOCAL	Calibrate VCOs whenever registers h05 and h06 are written.
CAL	Start VCO calibration (auto clears).
MC0[1:0]	Setting to h1 mutes OUT0 output during calibration.
MC1[1:0]	Setting to h1 mutes OUT1 output during calibration.
MC2[1:0]	Setting to h1 mutes OUT2 output during calibration.
MC3[1:0]	Setting to h1 mutes OUT3 output during calibration.
MC4[1:0]	Setting to h1 mutes OUT4 output during calibration.

VCO Automatic Level Control (ALC)

The VCO uses an internal automatic level control (ALC) algorithm to maintain an optimal amplitude on the VCO resonator, and thus optimal phase noise performance. The user has several ALC configuration and status reporting options as seen in Table 13.

Table 13. ALC Bit Descriptions

BIT	DESCRIPTION
ALCCAL	Auto enable ALC during CAL operation.
ALCEN	Always enable ALC (overrides ALCCAL, ALCMON, and ALCULOK).
ALCHI	ALC too high flag (resonator amplitude too high).
ALCLO	ALC too low flag (resonator amplitude too low).
ALCMON	Enable amplitude monitoring for status flags only; does NOT enable ALC.
ALCULOK	Auto enable ALC when PLL unlocked.

Changes in the internal ALC output can cause extremely small jumps in the VCO frequency. These jumps may be acceptable in some applications but not in others. Use the above table to choose when the ALC is active. The ALCHI and ALCLO flags, valid only when the ALC is active or the ALCMON bit is set, may be used to monitor the resonator amplitude.

The ALC must be allowed to operate during or after a calibration cycle. At least one of the ALCCAL, ALCEN, or ALCULOK bits must be set.

OPERATION

VCO DIVIDER (N)

The 10-bit N divider provides the feedback from the VCO to the PFD. The divide ratio may be programmed from 32 to 1023, when bit RAO = 0. The divide ratio may be programmed from 2 to 511, when bit RAO = 1. Use the ND[9:0] bits found in registers h05 and h06 to directly program the N divide ratio. See the Applications Information section for the relationship between N and the f_{REF}, f_{PFD}, f_{VCO} and f_{OUTx} frequencies.

VCO PRESCALER (P)

The P divider reduces the VCO frequency and distributes it to the five output dividers. The available divide ratios of 2, 2.5, 3, 3.5 and 4, when coupled with the VCO frequency range, allow the P divider output to cover more than an octave of frequency. See Table 14 for programming specifics and the Applications Information section for the relationship between P and the f_{REF}, f_{PFD}, f_{VCO} and f_{OUTx} frequencies.

Table 14. PD[2:0] Programming

PD[2:0]	P
0	2
1	2.5
2	3
3	3.5
4	4
5 to 7	Invalid

OUTPUT DIVIDERS (M0, M1, M2, M3, M4)

The five independent output dividers are driven by the P divider. All settings of Mx ≥ 2 with any P value or Mx = 1 with P = 2, 3, or 4 provide a 50% duty cycle at the output. Setting Mx = 1 with P = 2.5 or 3.5 is allowable, but will produce a signal with a non-50% duty cycle (40% and 57%, respectively) and a large subharmonic spurious output. In systems where the LTC6951 output drives into a frequency divider of at least 2 (as in some ADCs), the subharmonic spur will be removed and the duty cycle will go to 50% at the frequency divider output.

The relationship between the Mx value and the MDx[3:0] bits is shown in Table 15. Unused dividers can be powered down to save current by setting the MCx[1:0] bits to 3. The description of the MCx[1:0] bits is shown in Table 16 and Table 17. Setting the bit RAO = 1 in register h03 causes the PLL to reconfigure with P, M0 and N as part of the overall VCO divide ratio to provide phase alignment between the outputs and the R divider output (f_{PFD}). See the Applications Information section for the relationship between M0, M1, M2, M3 and M4 and the f_{REF}, f_{PFD}, f_{VCO}, f_{OUT0}, f_{OUT1}, f_{OUT2}, f_{OUT3} and f_{OUT4} frequencies.

Table 15. MDx[3:0] Programming

MDx[3:0]	Mx
0	1
1	2
2	4
3	8
4	12
5	16
6	24
7	32
8	48
9	64
10	96
11	128
12	192
13	256
14	384
15	512

Table 16. MCx[1:0] Programming (x = 1 to 4)

MCx[1:0]	DESCRIPTION
0	Do not mute output on VCO CAL.
1	Mute output on VCO CAL.
2	Power down output (divider remains running and synchronized).
3	Power down divider and output.

Table 17. MC0[1:0] Programming

MC0[1:0]	DESCRIPTION
0	Do not mute output on VCO CAL.
1	Mute output on VCO CAL (RAO = 0). Power down output on VCO CAL (RAO = 1).
2	Power down output (divider remains running and synchronized).
3	Power down divider and output.

OPERATION

OUTPUT DELAYS (D0, D1, D2, D3, D4)

Each output divider can have the start time of the output delayed by integer multiples of the P divider output period during a synchronization event. The delay value Dx is programmed into the registers DLY0[7:0], DLY1[7:0], DLY2[7:0], DLY3[7:0] and DLY4[7:0] and can be any value from 0 to 255. Delays are only enabled with synchronization bits SYNCEN0, SYNCEN1, SYNCEN2, SYNCEN3 and SYNCEN4 set to "1". D0 is not available when bit RAO is set to "1". See the Operation section on Synchronization and the Applications Information section for details on the use of the delay settings.

CML OUTPUT BUFFERS (OUT0, OUT1, OUT2, OUT3)

Four of the outputs are very low noise, low skew 2.5V CML buffers. Each output can be AC- or DC-coupled and terminated with 100Ω differential. If a single-ended output is desired, each side of the CML output can be individually AC-coupled and terminated with 50Ω. The bits OINV0, OINV1, OINV2 and OINV3 can selectively invert the sense of each output to facilitate board routing without having to cross matched impedance traces. The bits MUTE0, MUTE1, MUTE2 and MUTE3 set the selected output to a logic "0" state with logic "0" sense set by the OINVx bits as shown in Table 18. (If bit RAO = 1, MUTE0 = 1 has no effect. Set MC0[1:0] = 2 to stop OUT0 from transitioning if RAO = 1.) To save power with the dividers running, each buffer can be turned off by setting the bits MC0[1:0], MC1[1:0], MC2[1:0], and MC3[1:0] to 2. See Figure 9 for circuit details and the Applications Information section for common interface configurations.

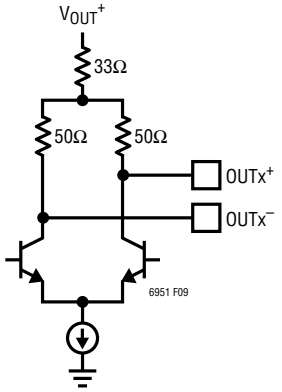


Figure 9. Simplified CML Interface Schematic (OUT0, OUT1, OUT2, OUT3)

LVDS OUTPUT BUFFER (OUT4)

The fifth output is a low noise LVDS buffer capable of operation up to 800MHz. This output is DC-coupled and terminated with 100Ω differential. The bit OINV4 can selectively invert the sense of the output to facilitate board routing without having to cross matched impedance traces. The bit MUTE4 sets the selected output to a logic "0" state with logic "0" sense set by the OINV4 bit as shown in Table 18. To save power with the dividers running, the buffer can be turned off by setting the bits MC4[1:0] to 2. See Figure 10 for circuit details and the Applications Information section for common interface configurations.

Table 18. Output Sense with MUTEx = 1 and OINVx Programming (x = 0 to 4)

OINVx	OUTx+	OUTx–
0	0	1
1	1	0

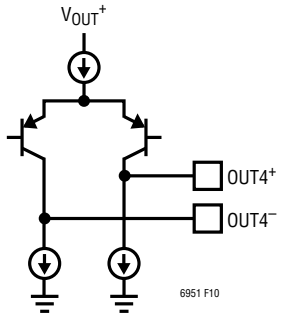


Figure 10. Simplified LVDS Interface Schematic (OUT4)

OUTPUT SYNCHRONIZATION (SYNC)

The LTC6951 has circuitry to allow the outputs to be synchronized into known phase alignment in several different ways to suit different applications using the EZSync and ParallelSync Multichip Clock Edge Synchronization protocols. Synchronization can be between any combination of outputs on the same chip (EZSync Standalone), across multiple cascaded follower chips (EZSync Multi-chip), or even across multiple parallel chips on the same reference domain (ParallelSync). Outputs can also be aligned to the REF input using the Reference Aligned Output mode (RAO = 1). Examples of EZSync standalone, EZSync multichip, and ParallelSync synchronization are shown in the

OPERATION

Applications Information section. The LTC6951Wizard Software Design Tool also provides graphical examples of these synchronization methods. For more information about the EZSync and ParallelSync Protocols, see the LTC6951 Synchronization Guide or contact the factory.

At initial power-up, after a POR, or any time output dividers M0, M1, M2, M3 or M4 are changed, the outputs will not be synchronized. Any changes to the output delays D0, D1, D2, D3 and D4 will not be reflected until after synchronization. Although the part will run properly and the outputs will be at the proper frequency without synchronization, it is highly recommended to use some form of synchronization. See Table 19 for descriptions of the applicable serial port bits and the Applications Information section for specific programming examples.

Table 19. SYNC Bit Descriptions

BIT	DESCRIPTION
DLY0[7:0]	D0 delay setting for the M0 divider (RAO = 0).
DLY1[7:0]	D1 delay setting for the M1 divider.
DLY2[7:0]	D2 delay setting for the M2 divider.
DLY3[7:0]	D3 delay setting for the M3 divider.
DLY4[7:0]	D4 delay setting for the M4 divider.
RAO	Reference alignment mode.
SN	SYNC pin falling edge time alignment to REF (RAO = 1); SSYNC ignored.
SR	SYNC pin rising edge time alignment of R divider to REF (RAO = 1); SSYNC ignored.
SSYNC	Software synchronization.
SYNCEN0	Enable synchronization of the M0 divider (RAO = 0).
SYNCEN1	Enable synchronization of the M1 divider.
SYNCEN2	Enable synchronization of the M2 divider.
SYNCEN3	Enable synchronization of the M3 divider.
SYNCEN4	Enable synchronization of the M4 divider.

Reference Aligned Output Mode (RAO)

The RAO bit (register h03) controls the fundamental configuration of the PLL and the ability to align the outputs back to the Reference input. Figure 3 shows the PLL loop diagram with bit RAO set to “0” which is the default power-up.

Figure 4 shows the PLL loop diagram with bit RAO set to “1”. The P and M0 dividers are now part of the overall feedback loop, and the range on the N divider has changed. SYNCEN0 has no effect on OUT0. DLY0[7:0] in register h0A is now inactive and the contents of h0A[7] and h0A[6] become SN and SR, respectively. See Table 5 for SN and SR function descriptions.

The N divider output is used as a timing event for all synchronization modes. Only when the P and M0 dividers are in the feedback loop can the output rising edges be coincident with the N divider output, and by inference the R divider output, creating a known and repeatable alignment between the outputs and the Reference input.

Synchronization Events

Synchronization begins either with the SYNC pin driven high or by writing “1” to the SSYNC bit (unless RAO = 1 and SR or SN = 1, in which case the SSYNC bit is inactive). Internal to the LTC6951, the SYNC pin’s signal and the SSYNC bit are logically ORed. Choose either the SYNC pin or the SSYNC bit for use during a synchronization event and keep the unused signal held at logic low. Any output with a valid SYNCENx bit set will stop running and return to a logic “0” state after an internal timing delay of greater than 100µs. The SYNC pin or SSYNC bit must remain high for a minimum of 1ms.

When bits RAO and SR are set to “1” and the SYNC pin is driven high, the R divider for R ≥ 2 is retimed as shown in Figure 5 and explained in the Reference Divider (R) section.

When the SYNC pin is driven back low, or “0” is written to the SSYNC bit in cases when it is active, internal retiming begins immediately to allow synchronized outputs to start again. One N divider cycle and then 18 P divider cycles are required to synchronize each output divider. A Dx delay setting of “0” causes that output to start immediately after the 18 P divider cycles. All synchronized outputs with the same Dx delay setting will have the output rising edge occur within the skew times as defined in the Electrical Characteristics table. The range on each delay is 0 to 255 P cycles and is independent of the Mx divide ratio setting of each divider.

OPERATION

The internal synchronization signal is controlled by the settings of RAO and SN. If either bit is "0" the internal synchronization falling edge is delayed by at least 25µs to meet the requirements of EZSync.

RAO = SN = 1, R = 1

When bits RAO and SN are "1", the value of R = 1 and the SYNC pin driven synchronously to the REF inputs, the output timing is as shown in Figure 11.

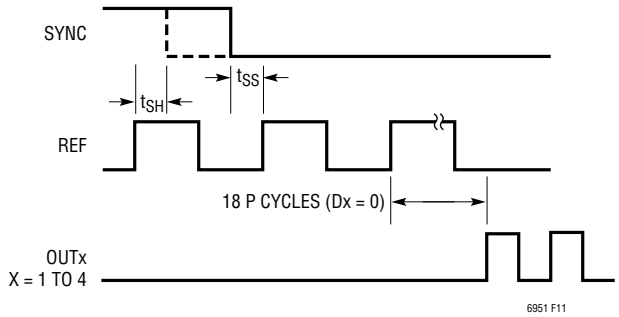


Figure 11. SYNC to REF timing (RAO = SN = 1, R = 1)

RAO = SN = SR = 1, R ≥ 2

When R ≥ 2 bits RAO, SN and SR are "1" and the SYNC pin is driven synchronously to the REF inputs, the output timing is as shown in Figure 12. Note the outputs are now retimed to the R divider output (R DIV) which is an internal node not accessible outside of the part. The SYNC timing must still meet setup (t_{SS}) and hold (t_{SH}) timing to REF. Combining Figure 12 with Figure 5 allows the ability to calculate the width of the SYNC pulse in terms of REF periods (REFCYCLES) to get precise timing back to R DIV with R ≥ 2, noting that the SYNC pulse needs to be high a minimum of 1ms.

$$REFCYCLES = R \bullet CEILING\left(\frac{1ms \bullet f_{REF}}{R}\right) + 1 \qquad (2)$$

where the CEILING(x) function returns the smallest integer greater than or equal to x.

Using Equation 2 to calculate the width of the SYNC pulse in terms of REFCYCLES is not required to get the outputs properly synchronized to each other or across multiple LTC6951s. However, the latency from REF to any output has R different possibilities depending on where SYNC falls relative to R DIV.

If the controlling system can make the SYNC pulse exactly REFCYCLES wide, all outputs will occur with the exact same latency to REF every time synchronization occurs. Note that Equation 2 calculates the minimum number of REFCYCLES for the SYNC pulse. Adding R multiples will give the same result. See ParallelSync Multi-Chip Synchronization in the Applications Information section for an example.

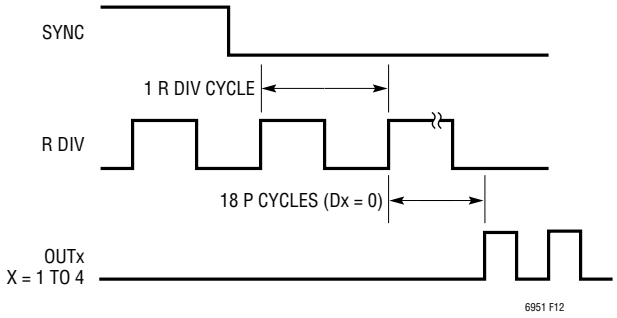


Figure 12. SYNC to R DIV timing (RAO = SN = SR = 1, R ≥ 2)

See Reference Signal and Sync Timing for SR and SN Modes in the Applications Information section for the timing requirements of SYNC to REF in this mode.

OPERATION

SERIAL PORT

The SPI-compatible serial port provides control and monitoring functionality. A configurable status output STAT gives additional instant monitoring.

Communication Sequence

The serial bus is composed of $\overline{CS}$, SCLK, SDI, and SDO. Data transfers to the part are accomplished by the serial bus master device first taking $\overline{CS}$ low to enable the LTC6951's port. Input data applied on SDI is clocked on the rising edge of SCLK, with all transfers MSB first. The communication burst is terminated by the serial bus master returning $\overline{CS}$ high. See Figure 13 for details.

Data is read from the part during a communication burst using SDO. Readback may be multidrop (more than one LTC6951 connected in parallel on the serial bus), as SDO is three-stated (Hi-Z) when $\overline{CS}$ is high, or when data is not being read from the part. *If the LTC6951 is not used in a multidrop configuration, or if the serial port master is not capable of setting the SDO line level between read sequences, it is recommended to attach a high-value resistor of greater than 200kΩ between SDO and GND to ensure the line returns to a known level during Hi-Z states.* See Figure 14 for details.

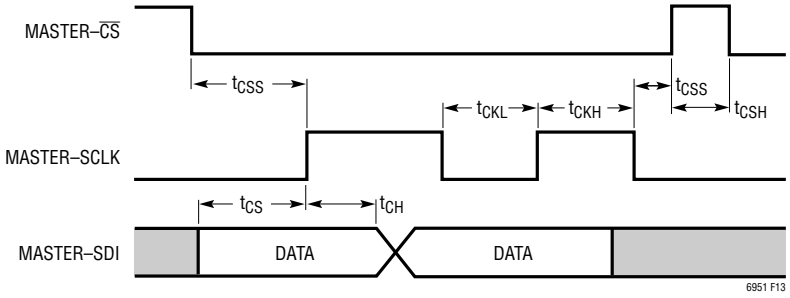


Figure 13. Serial Port Write Timing Diagram

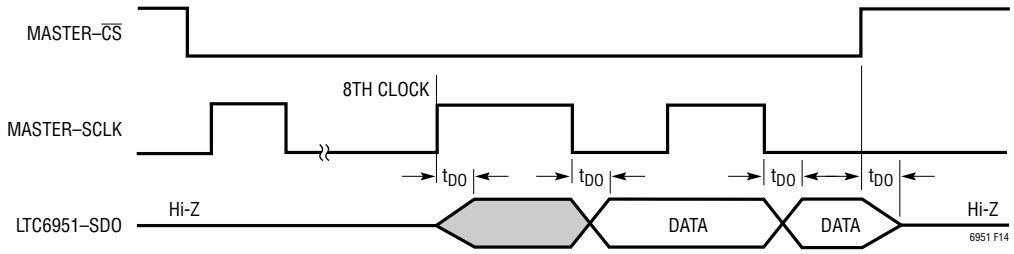


Figure 14. Serial Port Read Timing Diagram

OPERATION

Single Byte Transfers

The serial port is arranged as a simple memory map, with status and control available in 20, byte-wide registers. All data bursts are comprised of at least two bytes. The 7 most significant bits of the first byte are the register address, with an LSB of 1 indicating a read from the part, and LSB of 0 indicating a write to the part. The subsequent byte, or bytes, is data from/to the specified register address. See Figure 15 for an example of a detailed write sequence, and Figure 16 for a read sequence.

Figure 17 shows an example of two write communication bursts. The first byte of the first burst sent from the serial bus master on SDI contains the destination register address (ADDRX) and an LSB of "0" indicating a write. The next byte is the data intended for the register at address ADDRX. $\overline{CS}$ is then taken high to terminate the transfer. The first byte of the second burst contains the destination register address (ADDRY) and an LSB indicating a write. The next byte on SDI is the data intended for the register at address ADDRY. $\overline{CS}$ is then taken high to terminate the transfer.

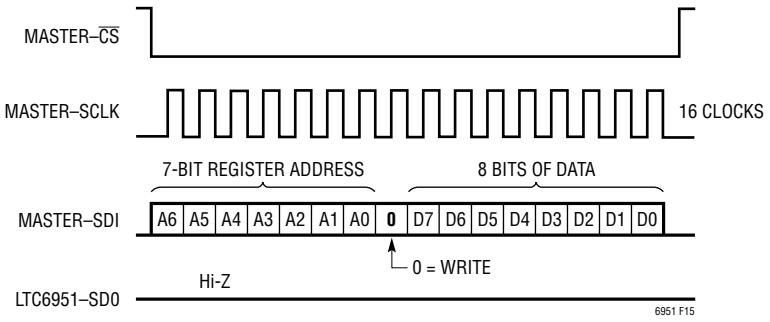


Figure 15. Serial Port Write Sequence

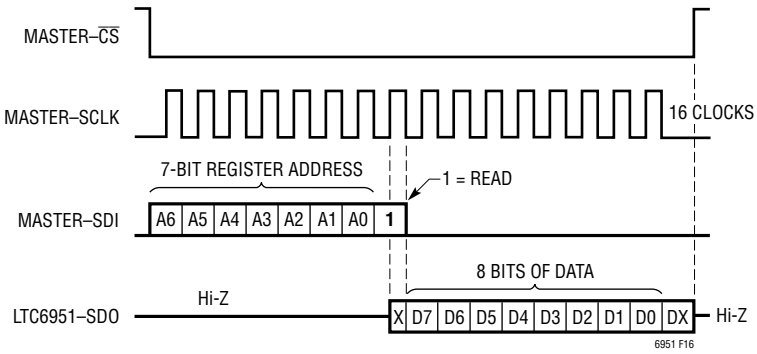


Figure 16. Serial Port Read Sequence

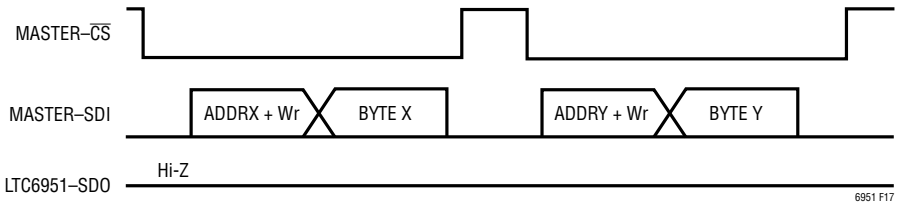


Figure 17. Serial Port Single Byte Writes

OPERATION

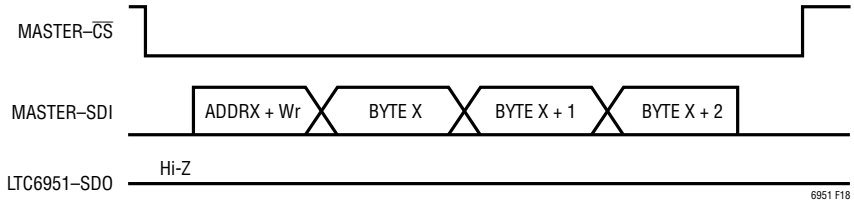


Figure 18. Serial Port Auto-Increment Write

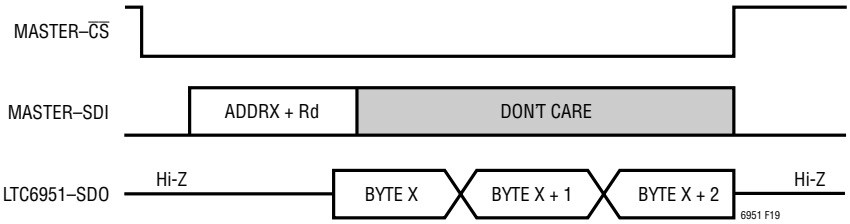


Figure 19. Serial Port Auto-Increment Read

Multiple Byte Transfers

More efficient data transfer of multiple bytes is accomplished by using the LTC6951's register address auto-increment feature as shown in Figure 18. The serial port master sends the destination register address in the first byte and its data in the second byte as before, but continues sending bytes destined for subsequent registers. Byte 1's address is ADDRX+1, Byte 2's address is ADDRX+2, and so on. If the register address pointer attempts to increment past 19 (h13), it is automatically reset to 0.

An example of an auto-increment read from the part is shown in Figure 19. The first byte of the burst sent from the serial bus master on SDI contains the destination register address (ADDRX) and an LSB of "1" indicating a read. Once the LTC6951 detects a read burst, it takes SDO out of the Hi-Z condition and sends data bytes sequentially, beginning with data from register ADDRX. The part ignores all other data on SDI until the end of the burst.

Multidrop Configuration

Several LTC6951s may share the serial bus. In this multidrop configuration, SCLK, SDI, and SDO are common between all parts. The serial bus master must use a separate $\overline{CS}$ for each part and ensure that only one device has $\overline{CS}$ asserted at any time. It is recommended to attach a high-value resistor to SDO to ensure the line returns to a known level during Hi-Z states.

OPERATION

Serial Port Registers

The memory map of the LTC6951 may be found below in Table 20, with detailed bit descriptions found in Table 21. The register address shown in hexadecimal format under the "ADDR" column is used to specify each register. Each register is denoted as either read-only (R) or read-write (R/W). The register's default value on device power-up or after a reset is shown at the right.

The read-only register at address h00 is used to determine different status flags. These flags may be instantly output on the STAT pin by configuring register h01. See STAT Output section below for more information.

The register at address h13 is a read-only byte for device identification.

Table 20. Serial Port Register Contents

ADDR	MSB	[6]	[5]	[4]	[3]	[2]	[1]	LSB	R/W	DEFAULT
h00	*	UNLOCK	ALCHI	ALCLO	$\overline{\text{LOCK}}$	LOCK	$\overline{\text{REFOK}}$	REFOK	R	
h01	INVSTAT	x[6]	x[5]	x[4]	x[3]	x[2]	x[1]	x[0]	R/W	h8A
h02	PDALL	PDPLL	PDVCO	PDOUT	PDREFPK	SSYNC	POR	CAL	R/W	h00
h03	ALCEN	ALCMON	ALCCAL	ALCULOK	AUTOCAL	RAO	BST	FILT	R/W	h3A
h04	BD[3]	BD[2]	BD[1]	BD[0]	*	LKWIN	LKCT[1]	LKCT[0]	R/W	h93
h05	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	ND[9]	ND[8]	R/W	h04
h06	ND[7]	ND[6]	ND[5]	ND[4]	ND[3]	ND[2]	ND[1]	ND[0]	R/W	h28
h07	CPMID	CPWIDE	CPRST	CPUP	CPDN	CP[2]	CP[1]	CP[0]	R/W	hA7
h08	PD[2]	PD[1]	PD[0]	MUTE4	MUTE3	MUTE2	MUTE1	MUTE0	R/W	h60
h09	SYNCEN0	OINV0	MC0[1]	MC0[0]	MD0[3]	MD0[2]	MD0[1]	MD0[0]	R/W	h92
h0A (RAO = 0) (RAO = 1)	DLY0[7] SN	DLY0[6] SR	DLY0[5] *	DLY0[4] *	DLY0[3] *	DLY0[2] *	DLY0[1] *	DLY0[0] *	R/W R/W	h00 h00
h0B	SYNCEN1	OINV1	MC1[1]	MC1[0]	MD1[3]	MD1[2]	MD1[1]	MD1[0]	R/W	h92
h0C	DLY1[7]	DLY1[6]	DLY1[5]	DLY1[4]	DLY1[3]	DLY1[2]	DLY1[1]	DLY1[0]	R/W	h00
h0D	SYNCEN2	OINV2	MC2[1]	MC2[0]	MD2[3]	MD2[2]	MD2[1]	MD2[0]	R/W	h92
h0E	DLY2[7]	DLY2[6]	DLY2[5]	DLY2[4]	DLY2[3]	DLY2[2]	DLY2[1]	DLY2[0]	R/W	h00
h0F	SYNCEN3	OINV3	MC3[1]	MC3[0]	MD3[3]	MD3[2]	MD3[1]	MD3[0]	R/W	h92
h10	DLY3[7]	DLY3[6]	DLY3[5]	DLY3[4]	DLY3[3]	DLY3[2]	DLY3[1]	DLY3[0]	R/W	h00
h11	SYNCEN4	OINV4	MC4[1]	MC4[0]	MD4[3]	MD4[2]	MD4[1]	MD4[0]	R/W	h8B
h12	DLY4[7]	DLY4[6]	DLY4[5]	DLY4[4]	DLY4[3]	DLY4[2]	DLY4[1]	DLY4[0]	R/W	h00
h13	REV[3]	REV[2]	REV[1]	REV[0]	PART[3]	PART[2]	PART[1]	PART[0]	R	hX1†

* unused.
† varies depending on revision.

OPERATION

Table 21. Serial Port Register Bit Field Summary

BITS	DESCRIPTION	DEFAULT	ADDR
ALCCAL	Auto enable ALC during CAL operation	1	h03
ALCEN	Always enable ALC (override)	0	h03
ALCHI	ALC too high flag		h00
ALCLO	ALC too low flag		h00
ALCMON	Enable ALC monitor for status flags only	0	h03
ALCULOK	Enable ALC when PLL unlocked	1	h03
AUTOCAL	Calibrate VCOs whenever registers h05 to h06 are written	1	h03
BD[3:0]	Calibration B divider value	h9	h04
BST	REF buffer boost current	1	h03
CAL	Start VCO calibration (auto clears)	0	h02
CP[2:0]	CP output current	h7	h07
CPDN	Force CP pump down	0	h07
CPMID	CP bias to mid-rail	1	h07
CPRST	CP Hi-Z	1	h07
CPUP	Force CP pump up	0	h07
CPWIDE	Extend CP pulse width	0	h07
DLY0[7:0]	D0 Delay for M0 Divider (RAO = 0)	h00	h0A
DLY1[7:0]	D1 Delay for M1 Divider	h00	h0C
DLY2[7:0]	D2 Delay for M2 Divider	h00	h0E
DLY3[7:0]	D3 Delay for M3 Divider	h00	h10
DLY4[7:0]	D4 Delay for M4 Divider	h00	h12
FILT	REF input buffer filter	0	h03
INVSTAT	Invert STAT output	1	h01
LKCT[1:0]	PLL lock cycle count	h3	h04
LKWIN	PLL lock indicator window	0	h04
LOCK	PLL lock indicator flag		h00
$\overline{\text{LOCK}}$	PLL lock indicator flag inverted		h00
MC0[1:0]	M0 Divider power control	h1	h09
MC1[1:0]	M1 Divider power control	h1	h0B
MC2[1:0]	M2 Divider power control	h1	h0D
MC3[1:0]	M3 Divider power control	h1	h0F
MC4[1:0]	M4 Divider power control	h0	h11
MD0[3:0]	M0 Divider value	h2	h09
MD1[3:0]	M1 Divider value	h2	h0B
MD2[3:0]	M2 Divider value	h2	h0D
MD3[3:0]	M3 Divider value	h2	h0F
MD4[3:0]	M4 Divider value	hB	h11
MUTE0	Mute OUT0 (only valid if RAO = 0)	0	h08
MUTE1	Mute OUT1	0	h08
MUTE2	Mute OUT2	0	h08
MUTE3	Mute OUT3	0	h08
MUTE4	Mute OUT4	0	h08
ND[9:0]	N Divider value	h028	h05, h06
OINV0	OUT0 inversion	0	h09
OINV1	OUT1 inversion	0	h0B
OINV2	OUT2 inversion	0	h0D
OINV3	OUT3 inversion	0	h0F
OINV4	OUT4 inversion	0	h11
PART[3:0]	Part code	h1	h13
PD[2:0]	P Divider value	h3	h08
PDALL	Full chip power-down	0	h02
PDOUT	Powers down MDx, OUTx buffers, SYNC	0	h02
PDPLL	Powers down REF, R DIV, PFD, CP, N DIV	0	h02
PDREFPK	Powers down REF input signal detector	0	h02
PDVCO	Powers down VCO, N DIV, PD, MDx, OUTx buffers, SYNC	0	h02
POR	Force power-on-reset	0	h02
RAO	Reference Alignment to Output Mode	0	h03
RD[5:0]	R Divider value (RD[5:0] > 0)	h01	h05
REFOK	Reference valid flag		h00
$\overline{\text{REFOK}}$	Reference not valid flag		h00
REV[3:0]	Rev code		h13
SN	Synchronize to N Divider (RAO = 1)	0	h0A
SR	Synchronize to R Divider (RAO = 1)	0	h0A
SSYNC	Software SYNC	0	h02
SYNCEN0	Enable SYNC on OUT0 (RAO = 0)	1	h09
SYNCEN1	Enable SYNC on OUT1	1	h0B
SYNCEN2	Enable SYNC on OUT2	1	h0D
SYNCEN3	Enable SYNC on OUT3	1	h0F
SYNCEN4	Enable SYNC on OUT4	1	h11
UNLOCK	PLL unlock flag		h00
x[6:0]	STAT output OR mask	h0A	h01

OPERATION

STAT Output

The STAT output pin is configured with the x[6:0] bits and INVSTAT of register h01. These bits are used to bit-wise mask, or enable, the corresponding status flags of status register h00, according to Equation 3 and shown schematically in Figure 20. The result of this bit-wise Boolean operation is then output on the STAT pin.

$$\text{STAT} = (\textit{OR}\ (\text{Reg00[6:0]}\ \textit{AND}\ \text{Reg01[6:0]})) \text{ exclusive-OR INVSTAT} \quad (3)$$

For example, if the application requires STAT to go high whenever the ALCHI, ALCLO, or REFOK flags are set, then x[5], x[4], and x[0] should be set to "1", giving a register value of h31.

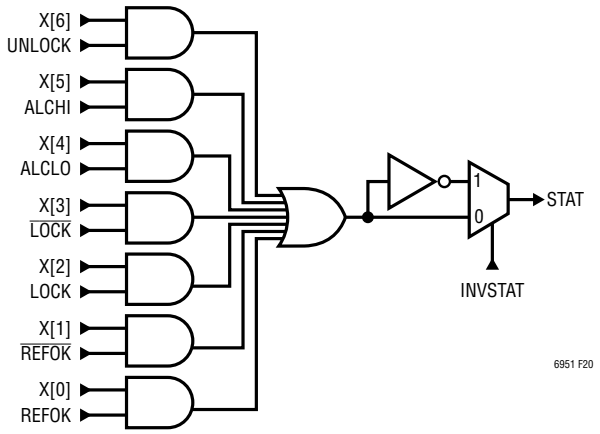


Figure 20. STAT Simplified Schematic

Block Power-down Control

The LTC6951's power-down control bits are located in register h02, described in Table 21. Different portions of the device may be powered down independently. To power down individual outputs, see Tables 16 and 17. *Care must be taken with bit[1] of the register, the POR (power-on-reset) bit. When written to "1", this bit forces a full reset of the part's digital circuitry to its power-up default state.*

APPLICATIONS INFORMATION

INTRODUCTION

A PLL is a complex feedback system that may conceptually be considered a frequency multiplier. The system multiplies the frequency input at REF± up to the VCO frequency. The PFD, charge pump, N divider, VCO, and external loop filter form a feedback loop to accurately control the VCO frequency (see Figure 21) when bit RAO = 0. The PFD, charge pump, N divider, P divider, M0 divider, VCO, and external loop filter form a feedback loop to accurately control the VCO frequency (see Figure 22) when bit RAO = 1. The R, P, M0, M1, M2, M3 and M4 dividers and input frequency f_{REF} are used to set the output frequency value and resolution.

The external loop filter is used to set the PLL's loop bandwidth, BW. Lower bandwidths generally have better spurious performance. Higher bandwidths can have better total integrated phase noise and lower integrated jitter.

OUTPUT FREQUENCY

When the loop is locked, the frequency f_{VCO} (in Hz) produced at the output of the VCO when RAO = 0 is determined by the reference frequency f_{REF}, and the R and N divider values, given by Equation 4:

$$f_{VCO} = \frac{f_{REF} \bullet N}{R} \quad (4)$$

When the loop is locked, the frequency f_{VCO} (in Hz) produced at the output of the VCO when RAO = 1 is determined by the reference frequency f_{REF}, and the R, N, P and M0 divider values, given by Equation 5:

$$f_{VCO} = \frac{f_{REF} \bullet N \bullet P \bullet M0}{R} \quad (5)$$

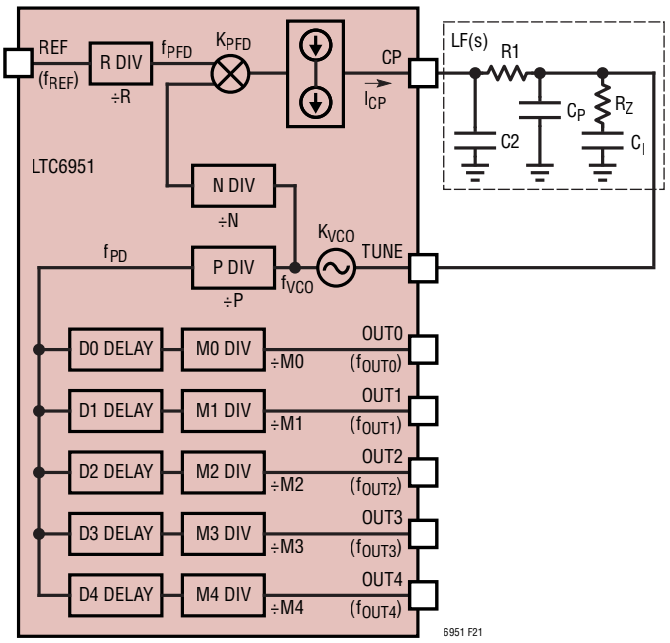


Figure 21. PLL Loop Diagram (RAO = 0)

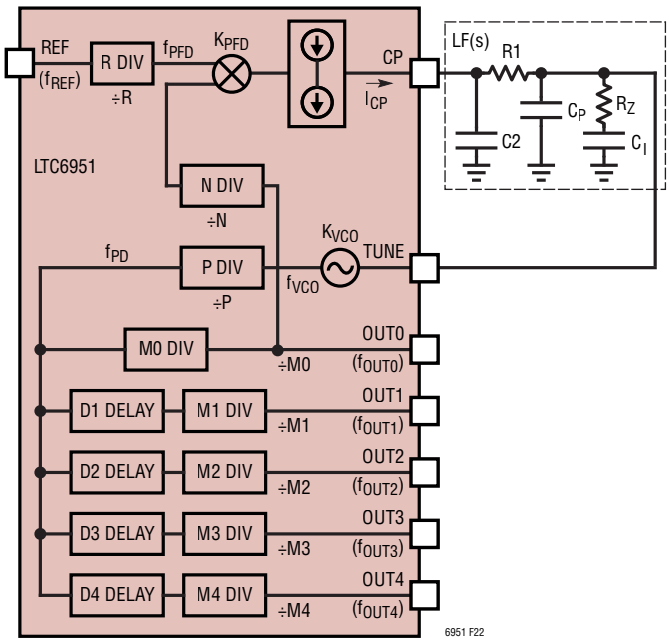


Figure 22. PLL Loop Diagram (RAO = 1)

APPLICATIONS INFORMATION

The PFD frequency f_{PFD} is given by the following equation:

$$f_{PFD} = \frac{f_{REF}}{R} \quad (6)$$

and f_{VCO} with RAO = 0 may be alternatively expressed as:

$$f_{VCO} = f_{PFD} \bullet N \quad (7)$$

and f_{VCO} with RAO = 1 may be alternatively expressed as:

$$f_{VCO} = f_{PFD} \bullet N \bullet P \bullet M0 \quad (8)$$

The output frequency f_{OUTx} produced at the output of the Mx dividers is given by Equation 9:

$$f_{OUTx} = \frac{f_{VCO}}{P \bullet Mx} \quad (9)$$

Using Equation 4 and Equation 9, the output frequency resolution f_{STEPx} produced by a unit change in N with RAO = 0 is given by Equation 10:

$$f_{STEPx} = \frac{f_{REF}}{R \bullet P \bullet Mx} \quad (10)$$

Using Equation 5 and Equation 9, the output frequency resolution f_{STEPx} produced by a unit change in N with RAO = 1 is given by Equation 11:

$$f_{STEPx} = \frac{f_{REF} \bullet M0}{R \bullet Mx} \quad (11)$$

OUTPUT DELAYS

Synchronization allows the start times of each output divider to be delayed by the value programmed into the delay registers and is expressed in P divider cycles. Applications needing to calculate the delay in terms of time can use Equation 12 where Dx is D0 to D4:

$$t_{Dx} = \frac{Dx \bullet P}{f_{VCO}} \quad (12)$$

LOOP FILTER DESIGN

A stable PLL system requires care in designing the external loop filter. The Linear Technology LTC6951Wizard application, available from http://www.linear.com/software/, aids in design and simulation of the complete system. Optimum phase noise and spurious performance can be obtained by using the third-order loop filter shown in Figures 20 and 21.

The loop design should use the following algorithm:

1) *Determine the output frequencies f_{OUTx} and the setting of RAO based on application requirements.* Using Equations 4 or 5, 6 and 9, change f_{REF}, N, R, P and Mx until the application frequency constraints are met. Use the minimum R value that still satisfies the constraints. Then calculate B using Table 10 or Table 11.

2) *Select the open loop bandwidth BW constrained by f_{PFD}.* A stable loop requires that BW is less than f_{PFD} by at least a factor of 10.

3) *Select loop filter component R_Z and charge pump current I_{CP} based on BW and the VCO gain factor, K_{VCO}.* BW (in Hz) is approximated by the following equation for RAO = 0:

$$BW \cong \frac{I_{CP} \bullet R_Z \bullet K_{VCO}}{2 \bullet \pi \bullet N} \quad (13)$$

or

$$R_Z = \frac{2 \bullet \pi \bullet BW \bullet N}{I_{CP} \bullet K_{VCO}}$$

or by the following equation for RAO = 1:

$$BW \cong \frac{I_{CP} \bullet R_Z \bullet K_{VCO}}{2 \bullet \pi \bullet N \bullet P \bullet M0} \quad (14)$$

or

$$R_Z = \frac{2 \bullet \pi \bullet BW \bullet N \bullet P \bullet M0}{I_{CP} \bullet K_{VCO}}$$

where K_{VCO} is in Hz/V, I_{CP} is in Amps, and R_Z is in Ohms. K_{VCO} is obtained from the VCO Tuning Sensitivity in the Electrical Characteristics. Use I_{CP} = 11.2mA to lower in-band noise unless component values force a lower setting.

APPLICATIONS INFORMATION

4) *Select loop filter components C_I, C_P, C_2 and R_1 based on BW and R_Z.* Use the following equations to calculate the remaining loop filter components.

$$C_I = \frac{4}{\pi \bullet BW \bullet R_Z} \quad (15)$$

$$C_P = \frac{1}{12 \bullet \pi \bullet BW \bullet R_Z} \quad (16)$$

$$C_2 = \frac{1}{18 \bullet \pi \bullet BW \bullet R_Z} \quad (17)$$

$$R_1 = R_Z \quad (18)$$

EZSync STANDALONE DESIGN AND PROGRAMMING EXAMPLE

This programming example uses the DC2248A with the LTC6951. Assume the following parameters of interest:

f_{REF} = 100MHz CMOS square wave

f_{OUT0} = 250MHz

f_{OUT1} = 250MHz in quadrature to f_{OUT0}

f_{OUT2} = 1GHz

f_{OUT3} = unused

f_{OUT4} = 125MHz

RAO = 0

From the Electrical Characteristics table:

f_{VCO} = 4.0GHz to 5.0GHz

$K_{VCO\%}$ = 2.5%Hz/V to 3.7%Hz/V

Determining Divider Values

Following the Loop Filter Design algorithm, first determine all the divider values. The maximum f_{PFD} is 100MHz, so R can be 1 noting that maximizing f_{PFD} in a data converter application will minimize integrated jitter.

R = 1

Then, using Equations 6 and 9 calculate the following values, preferably using the smallest P value for the solution:

P = 2

M0 = 8

M1 = 8

M2 = 2

M4 = 16

f_{PFD} = 100MHz

Then using Equation 7:

f_{VCO} = 4GHz

N = 40

Also, from Table 10 determine B:

B = 384 and BD[3:0] = hB

The same technique is used for the LTC6951-1, substituting f_{VCO} = 4.3GHz to 5.4GHz

Selecting Loop Bandwidth

The next step in the algorithm is choosing the open loop bandwidth. The maximum BW should be at least 10× smaller than f_{PFD}. Most data converter applications will place the bandwidth at the optimal intersection of VCO noise and in-band noise. Narrower bandwidths or higher order loop filters can be used to lower spurious power.

The LTC6951Wizard reports the thermal noise optimized loop bandwidth is 316kHz.

APPLICATIONS INFORMATION

Loop Filter Component Selection

Now set loop filter resistor R_Z and charge pump current I_{CP}. Because the K_{VCO} varies over the VCO's frequency range, using the K_{VCO} geometric mean gives good results:

$$K_{VCO} = 4.0 \bullet 10^9 \bullet \sqrt{0.025 \bullet 0.037}$$

$$= 121.7\text{MHz / V}$$

Using an I_{CP} of 11.2mA, the LTC6951Wizard uses Equation 13 to determine R_Z:

$$R_Z = 2 \bullet \pi \bullet 316k \bullet \frac{40}{11.2m \bullet 121.7M}$$

$$R_Z = 58.3\Omega$$

The LTC6951Wizard uses Equations 15 through 18 to calculate C_I, C_P, C_2 and R_1:

$$C_I = \frac{4}{\pi \bullet 316k \bullet 58.3} = 69.1\text{nF}$$

$$C_P = \frac{1}{12 \bullet \pi \bullet 316k \bullet 58.3} = 1.44\text{nF}$$

$$C_2 = \frac{1}{18 \bullet \pi \bullet 316k \bullet 58.3} = 0.96\text{nF}$$

$$R_1 = 58.3\Omega$$

Status Output Programming

This example will use the STAT pin to alert the system whenever the LTC6951 generates a fault condition. Program x[5], x[4], x[3], x[1] = 1 to force the STAT pin high whenever any of the ALCHI, ALCLO, $\overline{\text{LOCK}}$, or $\overline{\text{REFOK}}$ flags asserts:

Reg01 = h3A

Power Register Programming

For correct PLL operation all internal blocks should be enabled so the programmed state will be the same as the default value:

Reg02 = h00

VCO ALC, AUTOCAL, and Reference Input Settings Programming

Set the ALC options (ALCMON = ALCCAL = ALCULOK = 1), and the auto reset option (AUTOCAL = 1). The ALC will only be active during a calibration cycle or when the loop is unlocked, but the ALCHI and ALCLO status conditions will be monitored continuously. The VCO will be calibrated at the end of the SPI write communication burst (assuming an auto-increment write is used to write all registers).

From Table 1, FILT = 0 for a 100MHz reference frequency and BST = 0 for a CMOS square wave.

Now program Reg03, using the value RAO = 0 as stated in the programming example:

Reg03 = h78

Lock Detect Programming

Next, determine the lock indicator window from f_{PFD}. From Table 6 we see that LKWIN = 0 with a t_{LWW} of 5ns. The LTC6951 will consider the loop "locked" as long as the phase coincidence at the PFD is within 180°, as calculated below.

$$\text{phase} = 360° \bullet t_{LWW} \bullet f_{PFD} = 360 \bullet 5n \bullet 100M$$

$$\approx 180°$$

Choosing the correct COUNTS value depends upon the ratio of the bandwidth of the loop to the PFD frequency (BW/f_{PFD}) and the phase coincidence calculated above. Smaller ratios and larger phase coincidences dictate larger COUNTS values, although application requirements will vary. A COUNTS value of 2048 will work for this application. From Table 7, LKCT[1:0] = 3 for 2048 counts.

Use the LKCT[1:0] value from above, then use the previously determined BD[3:0] value to set Reg04:

Reg04 = hB3

APPLICATIONS INFORMATION

R and N Divider Programming

Program registers Reg05 to Reg06 with the previously determined R and N divider values. Because the AUTOCAL bit was previously set to 1, CAL in Reg02 does not need to be set:

Reg05 = h04

Reg06 = h28

Charge Pump Function and Current Programming

Disable all the charge pump functions (CPMID, CPWIDE, CPRST, CPUP, and CPDN), allowing the loop to lock. Using Table 8 with the previously selected I_{CP} of 11.2mA gives CP[2:0] = 7. This gives enough information to program Reg07:

Reg07 = h07

P Divider and Mute Programming

The P divider value was already determined and according to Table 14 sets PD[2:0] = h0. Each output divider has an individual MUTE function in this register. For now leave MUTE off and program Reg08:

Reg08 = h00

Output Divider, Delay and Function Programming

Two registers for each output allow the outputs to be configured independently of each other. The first register controls whether EZSync is enabled, whether the output is inverted, the CAL and power behavior from Table 16, and the output divide ratio from Table 15. The second register controls the delay values during an EZSync event and is only used if the SYNCENx bit of that output is set to a "1". To demonstrate the power of EZSync each used output will have synchronization enabled.

OUT0 with synchronization enabled, the output not inverted, set to mute on VCO CAL, and with M0 = 8 programs Reg09 to:

Reg09 = h93

OUT0 will be considered the reference output, so the delay, D0, will be set to 0:

Reg0A = h00

OUT1 with synchronization enabled, the output not inverted, set to mute on VCO CAL, and with M1 = 8 programs Reg0B to:

Reg0B = h93

OUT1 is defined to be in quadrature to OUT0. A 90° phase shift is ¼ of a cycle, therefore ¼ of M1 is 2; set D1 = 2:

Reg0C = h02

OUT2 with synchronization enabled, the output not inverted, set to mute on VCO CAL, and with M0 = 2 programs Reg0D to:

Reg0D = h91

OUT2 will be aligned to the reference output OUT0, so the delay, D2, will be set to 0:

Reg0E = h00

OUT3 is unused, so setting MC3[1:0] = 3 overrides the other values:

Reg0F = h30

Reg10 = h00

OUT4 with synchronization enabled, the output not inverted, set to mute on VCO CAL, and with M0 = 16 programs Reg11 to:

Reg11 = h95

OUT4 will be aligned to the reference output so the delay, D4, will be set to 0:

Reg12 = h00

Once all the registers defined above have been written and $\overline{CS}$ is driven back high, the part will initiate a CAL routine and the loop will lock. This can be monitored by reading Reg00 and waiting until LOCK = 1 or by observing the STAT pin going to a logic low.

APPLICATIONS INFORMATION

Synchronization

The outputs in this example are now running at the desired frequency, but have random phase relationships with each other. Synchronization forces the outputs to run at known and repeatable phases and can be achieved in this example either externally, by driving the SYNC pin, or internally, with the SSYNC bit in Reg02. Since the part was just programmed, use the SSYNC bit and hold the SYNC pin low:

Reg02 = h04

After waiting a minimum of 1ms, write Reg02 again:

Reg02 = h00

Once the internal synchronization process completes, the outputs will be aligned as shown in Figure 23.

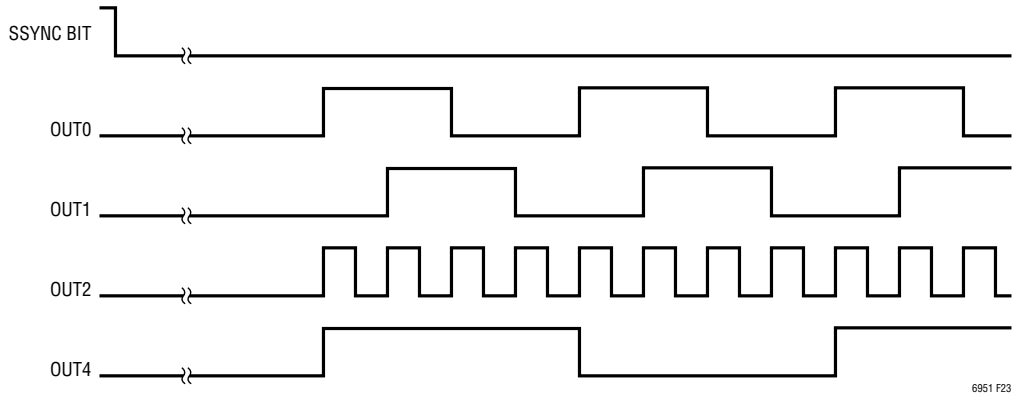


Figure 23. Outputs after SSYNC for the Design Example

APPLICATIONS INFORMATION

EZSync MULTI-CHIP SYNCHRONIZATION EXAMPLE

The LTC6951 conforms to the Linear Technology EZSync protocol Simple synchronization of multiple cascaded chips is accomplished by driving each chip's SYNC pin with a common CMOS signal. There are no precision timing requirements for this pulse as long as the SYNC skew to cascaded chips is less than 10µs and the SYNC high and low times are at least 1ms.

Since the LTC6951 is a clock generator, it is defined as a CONTROLLER for EZSync. Any EZSync part wired to any

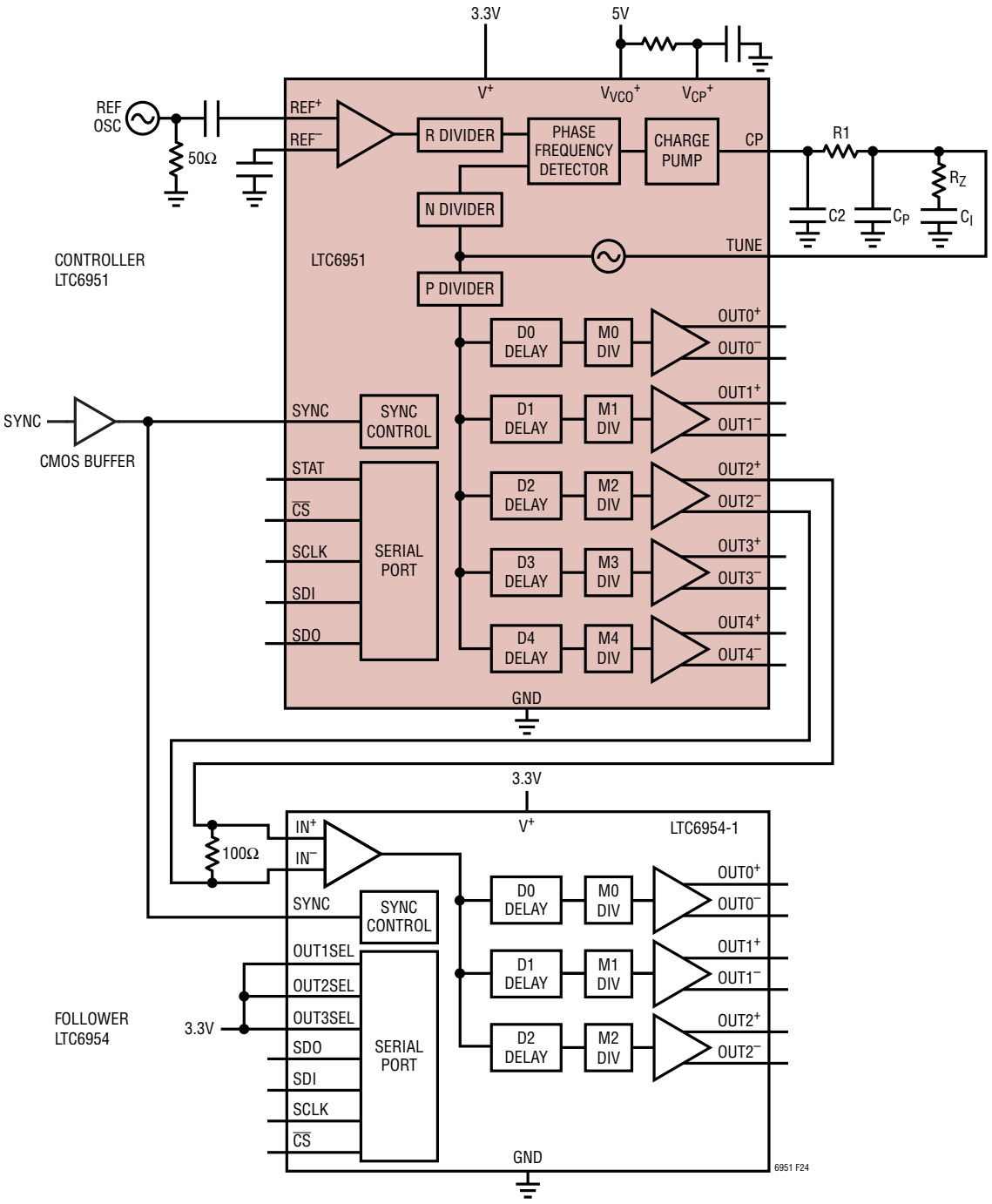


Figure 24. EZSync Multi-Chip Synchronization Design Example Block Diagram

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of the CONTROLLER's outputs, such as the LTC6950 or LTC6954, is defined as a FOLLOWER. Any CONTROLLER output driving a FOLLOWER is considered a follower-driver, and any CONTROLLER output which is synchronized to the FOLLOWER is considered follower-synchronous. See the LT Journal article about the LTC6950 (http://cds.linear.com/docs/en/lt-journal/LTJournal-V24N4-02-df-LTC6950-ChrisPearson.pdf) for a complete discussion of the EZSync protocol. This example will show how to program an LTC6951 as a CONTROLLER to an LTC6954-1 FOLLOWER wired as shown in Figure 24 and synchronize all outputs.

This programming example uses the LTC6951 and the LTC6954-1. Note that AC coupling capacitors are NOT allowed between the LTC6951 OUT2± outputs and the LTC6954-1 IN± inputs. Assume the following parameters of interest for the LTC6951:

f_{REF} = 100MHz CMOS square wave

f_{OUT0} = 250MHz

f_{OUT1} = 250MHz in quadrature to f_{OUT0}

f_{OUT2} = 1GHz routed to LTC6954-1

f_{OUT3} = unused

f_{OUT4} = 125MHz

RAO = 0

Assume the following parameters of interest for the LTC6954-1:

f_{IN} = 1GHz from LTC6951 OUT2

f_{OUT0} = 250MHz

f_{OUT1} = 250MHz

f_{OUT2} = 1GHz

Additionally the goal is for OUT0, OUT1 and OUT4 of the LTC6951 to be synchronized to OUT0, OUT1 and OUT2 of the LTC6954-1. EZSync defines OUT0, OUT1 and OUT4 of the LTC6951 as follower-synchronous and OUT2 of the LTC6951 as a follower-driver.

Determining Divider Values

This example uses the values found in the first example. Changes will be noted as needed. For the LTC6951:

R = 1

P = 2

M0 = 8

M1 = 8

M2 = 2

M4 = 16

f_{PFD} = 100MHz

N = 40

B = 384 and BD[3:0] = hB

For the LTC6954-1:

M0 = 4

M1 = 4

M2 = 1

Loop Filter Component Selection

This loop uses the same components as the previous example:

R_Z = 58.3Ω

C_I = 69.1nF

C_P = 1.44nF

C_2 = 0.96nF

R_1 = 58.3Ω

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LTC6951 Register Programming

Reg01 = h3A

Reg02 = h00

Reg03 = h78

Reg04 = hB3

Reg05 = h04

Reg06 = h28

Reg07 = h07

Reg08 = h00

Reg09 = h93

The delay settings are what the LTC6951 uses to implement each output's mode. OUT0, OUT1 and OUT4 are follower-synchronous and OUT2 is a follower-driver in this example. The LTC6954-1 requires 7 clock cycles on the input before the outputs will begin toggling. OUT2 as a follower-driver is defined with 0 delay as the reference point. All follower-synchronous outputs of the LTC6951 need to be delayed by 7 follower-driver clock cycles. The information needed to do this calculation are the divide ratio of the follower-driver (M_{FD}) and the desired delay of the output (Dx). The result of the equation below for each output is the follower-synchronous delay (D_{FSX}):

$$D_{FSX} = Dx + M_{FD} \bullet 7 \quad (19)$$

Using the above equation with M2 = M_{FD} = 2 and D0 = 0:

$D_{FS0} = 0 + 2 \bullet 7 = 14$

Therefore:

Reg0A = h0E

Reg0B = h93

With the desire for OUT1 to still be in quadrature to OUT0, use Equation 17 with D1 = 2:

$D_{FS1} = 2 + 2 \bullet 7 = 16$

Therefore:

Reg0C = h10

Reg0D = h91

The follower-driver delay, D2, is set to 0:

Reg0E = h00

Reg0F = h30

Reg10 = h00

Reg11 = h95

OUT4 is also follower-synchronous with D4 = 0:

$D_{FS4} = 0 + 2 \bullet 7 = 14$

Therefore:

Reg12 = h0E

Once all the registers defined above have been written and $\overline{CS}$ is driven back high, the part will initiate a CAL routine and the loop will lock. This can be monitored by reading Reg00 and waiting until LOCK = 1 or by observing the STAT pin going to a logic low.

LTC6954-1 Register Programming

Make sure the part is powered up:

Reg00 = h00

Set SYNC_EN0 = 1 and the delay for OUT0 = 0:

Reg01 = h80

Set the divide for OUT0 = 4:

Reg02 = h04

Set SYNC_EN1 = 1 and the delay for OUT1 = 0:

Reg03 = h80

Set the divide for OUT1 = 4:

Reg04 = h04

Set SYNC_EN2 = 1 and the delay for OUT2 = 0:

Reg05 = h80

Set the divide for OUT2 = 1:

Reg06 = h01

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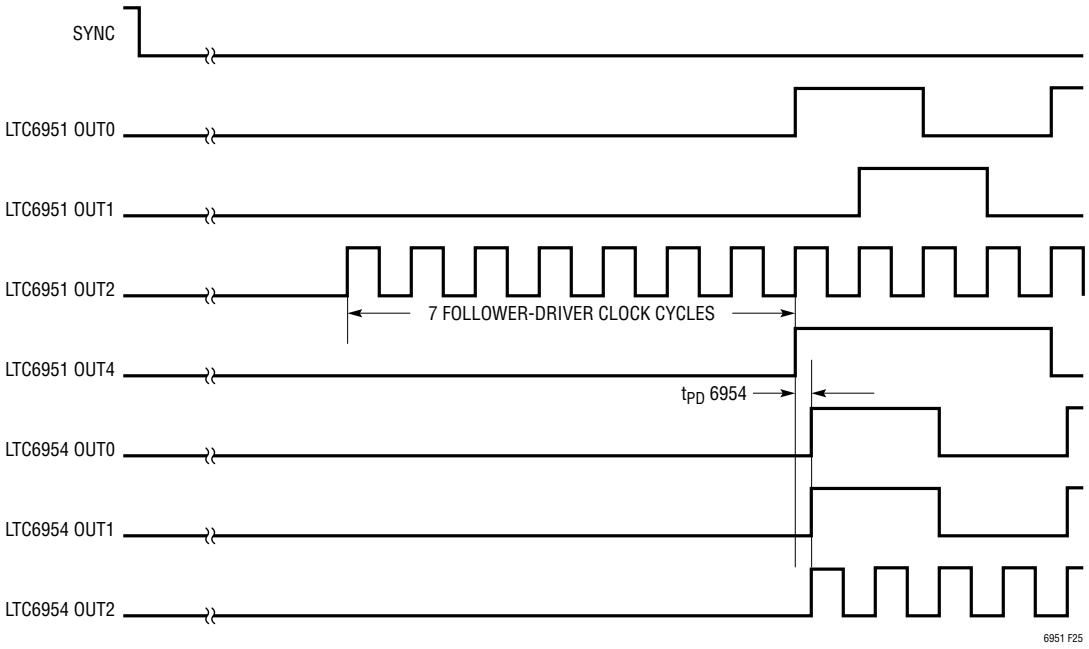

Figure 25. Outputs after SYNC for the EZSync Design Example

Synchronization

The outputs in this example are now running at the desired frequency, but have random phase relationships with each other. Synchronization forces the outputs to run at known and repeatable phases and can be achieved in this example by driving the SYNC pins of each part high for a minimum of 1ms and then driving the SYNC pins back low. The SYNC skew between parts can be as large as 10µs and still provide correct synchronization. Once the internal synchronization process completes, the outputs will be aligned as shown in Figure 25.

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ParallelSync MULTI-CHIP SYNCHRONIZATION EXAMPLE

Linear Technology's ParallelSync protocol is a method of synchronizing the outputs of multiple LTC6951s connected in parallel with a common reference. Parallel connection provides the best possible jitter performance since clock path cascading is not necessary to achieve synchronization. This method is also useful for applications using multiple LTC6951 daughter cards on a single reference backplane.

Using ParallelSync, all outputs across multiple LTC6951s are aligned not only in phase, but at initial start time as long as the system can provide the CMOS SYNC pulse synchronous to the reference input. To do this the LTC6951 needs to be put into Reference Aligned Output mode (bit

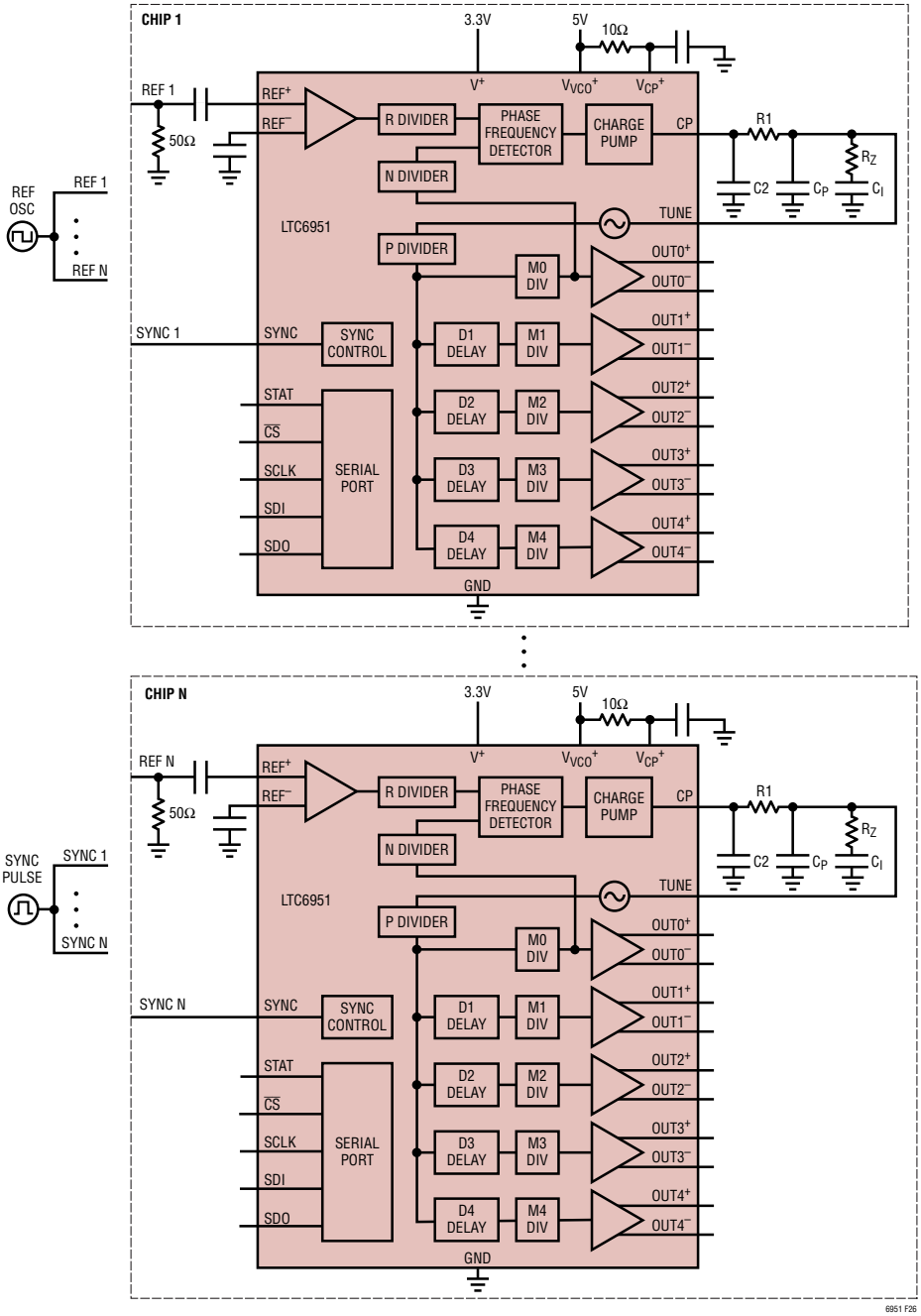

Figure 26. ParallelSync Multi-Chip Synchronization Design Example Block Diagram

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RAO), which reconfigures the loop as shown in Figure 22. This puts the P divider and M0 divider into the loop, allowing OUT0 to have edges coincident with the N divider and, by loop inference, to the R divider. This example will show how to program an LTC6951 and then use the SYNC pin to create outputs which will be aligned in phase and time for the system shown in Figure 26. The reference and SYNC inputs are split and sent to the individual chips. The number of parallel LTC6951s is only limited by the capability of the system to maintain accurate reference and SYNC timing.

This programming example uses multiple identically programmed LTC6951s. Assume the following parameters of interest:

f_{REF} = 100MHz CMOS square wave

f_{OUT0} = 250MHz

f_{OUT1} = 250MHz in quadrature to f_{OUT0}

f_{OUT2} = 500MHz

f_{OUT3} = unused

f_{OUT4} = 125MHz

RAO = 1

From the Electrical Characteristics table:

f_{VCO} = 4.0GHz to 5.0GHz

$K_{VCO\%}$ = 2.5%Hz/V to 3.7%Hz/V

Determining Divider Values

Following the Loop Filter Design algorithm, first determine all the divider values. Rearranging Equation 8 and Equation 9 gives the following:

$$f_{OUT0} = \frac{f_{REF} \bullet N}{R}$$

Since N and R must be integers, choose the smallest R that makes N an integer which is:

R = 2

Then, using Equations 6 and 9 calculate the following values, preferably using the smallest P value for the solution:

P = 2

M0 = 8

M1 = 8

M2 = 4

M4 = 16

f_{PFD} = 50MHz

Then using Equation 8:

N = 5

Also, from Table 11 determine B:

B = 256 and BD[3:0] = hA

The same technique is used for the LTC6951-1, substituting f_{VCO} = 4.3GHz to 5.4GHz.

Selecting Loop Bandwidth

The next step in the algorithm is choosing the open loop bandwidth. The maximum BW should be at least 10x smaller than f_{PFD}. Most data converter applications will place the bandwidth at the optimal intersection of VCO noise and in-band noise. Narrower bandwidths or higher order loop filters can be used to lower spurious power.

The LTC6951Wizard reports the thermal noise optimized loop bandwidth is 230kHz.

Loop Filter Component Selection

Now set loop filter resistor R_Z and charge pump current I_{CP}. Because the K_{VCO} varies over the VCO's frequency range, using the K_{VCO} geometric mean gives good results:

$$K_{VCO} = 4.0 \bullet 10^9 \bullet \sqrt{0.025 \bullet 0.037}$$

$$= 121.7MHz / V$$

Using an I_{CP} of 11.2mA, the LTC6951Wizard uses Equation 14 to determine R_Z:

$$R_Z = \frac{2 \bullet \pi \bullet 230k \bullet 5 \bullet 2 \bullet 8}{11.2m \bullet 121.7M}$$

$$R_Z = 84.8\Omega$$

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The LTC6951Wizard uses Equations 15 through 18 to calculate C_I, C_P, C_2 and R_1:

$$C_I = \frac{4}{\pi \bullet 230k \bullet 84.8} = 65.3nF$$

$$C_P = \frac{1}{12 \bullet \pi \bullet 230k \bullet 84.8} = 1.36nF$$

$$C_2 = \frac{1}{18 \bullet \pi \bullet 230k \bullet 84.8} = 0.91nF$$

$$R_1 = 84.8\Omega$$

Register Programming

Reg01 = h3A

Reg02 = h00

Write bit RAO = 1 and turn off AUTOCAL (the CAL bit must be set later):

Reg03 = h74

Set the new B value:

Reg04 = hA3

Write new R and N values:

Reg05 = h08

Reg06 = h05

Reg07 = h07

Reg08 = h00

The configuration of OUT0 in Reg09 changes with RAO = 1. Set SYNCEN0 = 0 since it is inactive:

Reg09 = h13

Reg0A with RAO = 1 now contains the bits SN and SR which control the synchronizing behavior. To do proper time alignment set SN = 1 and, since R ≥ 2, set SR = 1:

Reg0A = hC0

Reg0B = h93

OUT1 is defined to be in quadrature with OUT0, which from the previous examples is an initial delay of 2 (D1i = 2). Referring to Figure 11 shows the outputs do not start for 18 P cycles after an N divider retiming event. OUT0 always has a rising edge at the N divider in this mode, so OUT1 needs to be moved to the same spot with the delay settings. This is achieved by knowing how many P cycles are in one N cycle and subtracting 18. Use the following equation to find the correct delay noting Dxi is the desired initial delay:

$$Dx = Dxi + CEILING\left(\frac{18}{N \bullet M0}\right) \bullet N \bullet M0 - 18 \qquad (20)$$

where the CEILING(x) function returns the smallest integer greater than or equal to x.

In this example (with D1i = 2):

D1 = 2 + 1 • 5 • 8 – 18 = 24

Then program this delay into Reg0C:

Reg0C = h18

M2 = 4 which sets MD2[3:0] = h2:

Reg0D = h92

Equation 18 calculates D2 (and D4) as well with D2i and D4i set to 0:

D2 = D4 = 0 + 1 • 5 • 8 – 18 = 22

Write this into Reg0E (and Reg12 for OUT4):

Reg0E = h16

Reg0F = h30

Reg10 = h00

Reg11 = h95

Reg12 = h16

AUTOCAL has been turned off in this example. To properly calibrate the VCO the CAL bit must be set to “1”:

Reg02 = h01

The write to Reg02 to set the CAL bit must be done after all VCO or loop programming (R, N, P or M0). Once Reg02 has been written and $\overline{CS}$ is driven back high, the part will initiate a CAL routine and the loop will lock. This can be monitored by reading Reg00 and waiting until LOCK = 1 or by observing the STAT pin going to a logic low. The CAL bit self-clears once the calibration routine is finished.

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Synchronization

The outputs for all LTC6951s in this example are now running at the desired frequency, but have random phase relationships with each other. Synchronization across multiple LTC6951s requires a system master which can create a SYNC output synchronous to the REF signal, and then pass it to all LTC6951s while meeting setup and hold time requirements. Both edges of SYNC are used in this example to align the outputs. The rising edge allows the system to know the relationship between the REF input and the R divider output as shown in Figure 5. At this point all R divider outputs across multiple LTC6951s will have the same phase relationship.

Note that when SYNC is driven high in this case the loop will likely lose phase lock. As long as the loop bandwidth is well above 10kHz, the loop will be stabilized during the 1ms SYNC high time requirement.

To get repeatable REF-to-output latency with R ≥ 2, the SYNC pulse must be an exact number of REFCYCLES wide as described in Equation 2. *Note that this equation is only used for repeatable latency from REF to the outputs. Synchronization across all LTC6951s will still work without this calculation, but the latency will vary by R counts.*

$$REFCYCLES = 2 \bullet CEILING\left(\frac{1ms \bullet 100M}{2}\right) + 1$$

$$= 100,001$$

where the CEILING(x) function returns the smallest integer greater than or equal to x.

Once the SYNC pin is driven back low, the outputs of all LTC6951s used in the example will be aligned as shown in Figure 27.

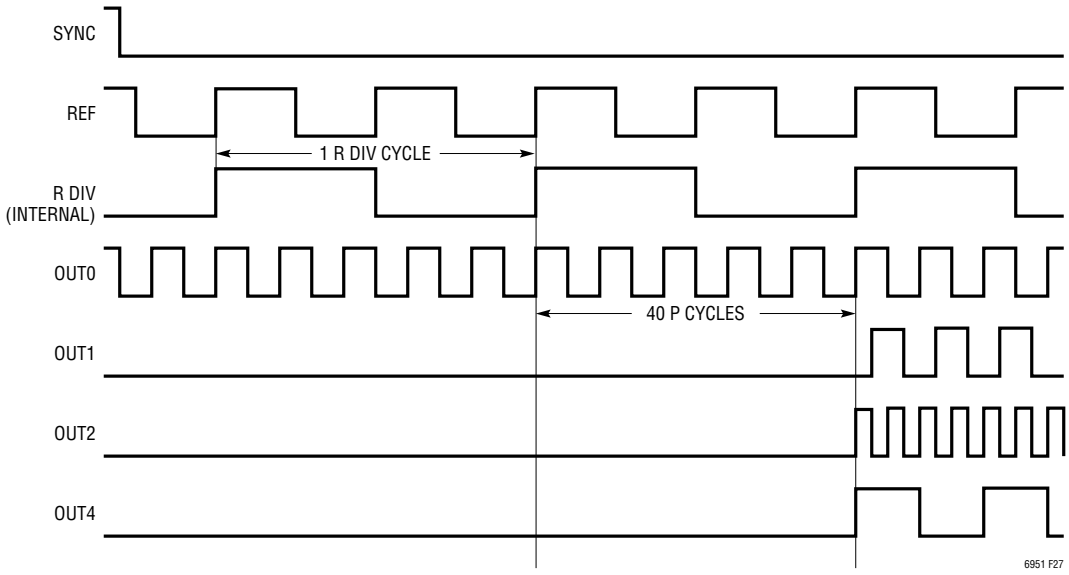

Figure 27. Outputs after SYNC for the ParallelSync Design Example

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JESD204B EXAMPLE

The JESD204B subclass 1 interface clocking can be accomplished with the LTC6951 as shown in the circuit example of Figure 28, utilizing two dual ADCs, an FPGA, and a 1:3 SYSREF buffer. In order to align multiple converter devices in time and provide repeatable and programmable latency across the serial link, the Local Multi-Frame Clocks (LMFC) and internal clock dividers on all devices in the system are synchronized by the pulse (or pulse train) SYSREF. Care must be taken to make sure the SYSREF signal remains synchronized to the ADC and FPGA clocks and meets setup and hold timing as specified by the devices.

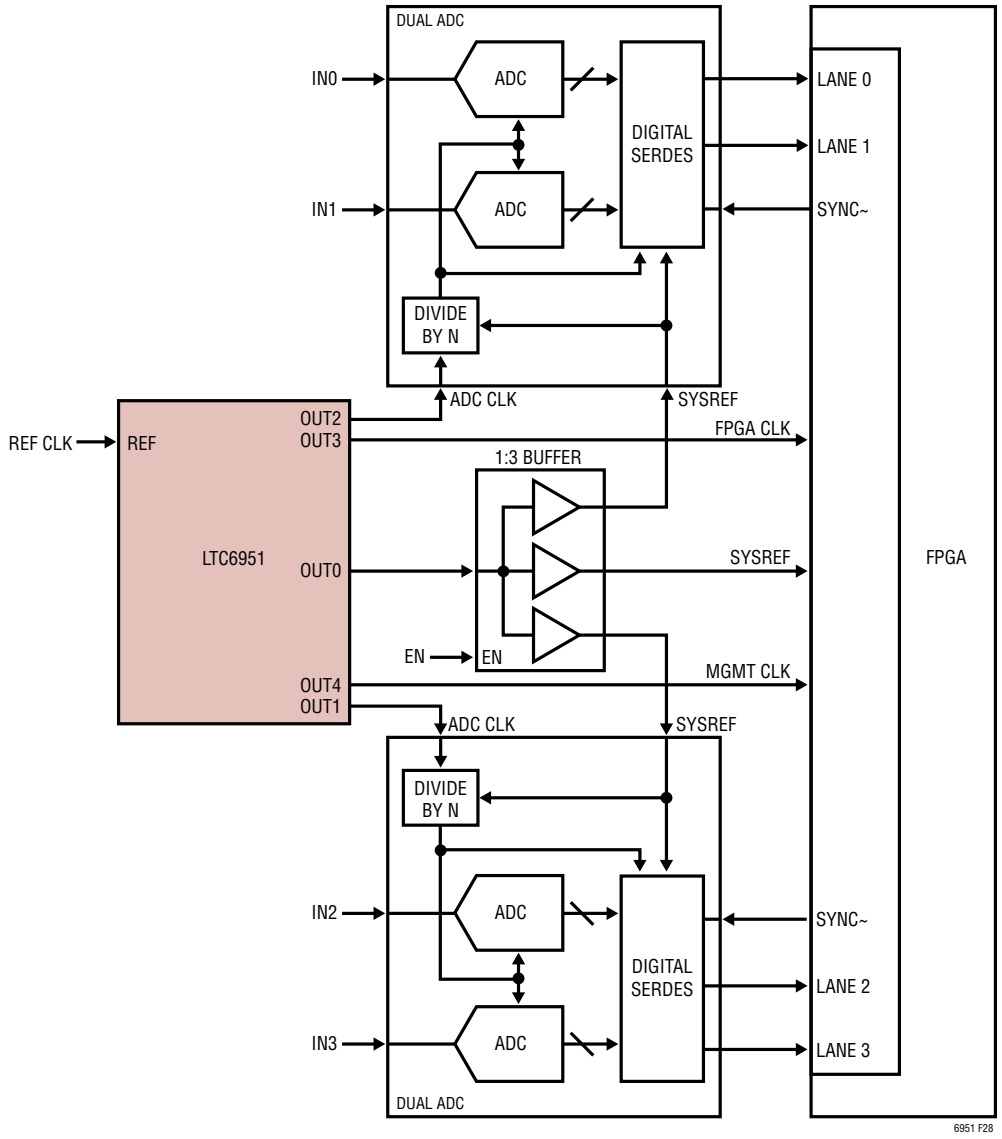

Figure 28. JESD204B Subclass 1 Design Example Block Diagram

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For this example assume the following parameters of interest:

f_{REF} = 61.44MHz @ 7dBm into 50Ω

$f_{OUT0} = f_{SYSREF}$ = 9.6MHz

$f_{OUT1} = f_{ADC}$ = 614.4MHz

$f_{OUT2} = f_{ADC}$ = 614.4MHz

$f_{OUT3} = f_{FPGA}$ = 153.6MHz

$f_{OUT4} = f_{MGMT}$ = 102.4MHz

RAO = 0

From the Electrical Characteristics table:

f_{VCO} = 4.0GHz to 5.0GHz

$K_{VCO\%}$ = 2.5%Hz/V to 3.7%Hz/V

Determining Divider Values

Following the Loop Filter Design algorithm, first determine all the divider values. The maximum f_{PFD} is 100MHz, so R can be 1 noting that maximizing f_{PFD} in a data converter application will minimize integrated jitter.

R = 1

Then, using Equations 6 and 9 calculate the following values for the LTC6951:

P = 2

M0 = 256

M1 = 4

M2 = 4

M3 = 16

M4 = 24

f_{PFD} = 61.44MHz

Then using Equation 7:

f_{VCO} = 4.9152GHz

N = 80

Also, from Table 10 determine B:

B = 256 and BD[3:0] = hA

The same technique is used for the LTC6951-1, substituting f_{VCO} = 4.3GHz to 5.4GHz.

Selecting Loop Bandwidth

The next step in the algorithm is choosing the open loop bandwidth. The maximum BW should be at least 10× smaller than f_{PFD}. Most data converter applications will place the bandwidth at the optimal intersection of VCO noise and in-band noise. Narrower bandwidths or higher order loop filters can be used to lower spurious power.

The LTC6951Wizard reports the thermal noise optimized loop bandwidth is 251kHz.

Loop Filter Component Selection

Now set loop filter resistor R_Z and charge pump current I_{CP}. Because the K_{VCO} varies over the VCO's frequency range, using the K_{VCO} geometric mean gives good results:

$$K_{VCO} = 4.9152 \cdot 10^9 \cdot \sqrt{0.025 \cdot 0.037}$$
$$= 149.5\text{MHz / V}$$

Using an I_{CP} of 11.2mA, the LTC6951Wizard uses Equation 13 to determine R_Z:

$$R_Z = \frac{2 \cdot \pi \cdot 251k \cdot 80}{11.2m \cdot 149.5M}$$

R_Z = 75.3Ω

The LTC6951Wizard uses Equations 15 and 16 to calculate C_I, C_P:

$$C_I = \frac{4}{\pi \cdot 251k \cdot 75.3} = 67.4\text{nF}$$

$$C_P = \frac{1}{12 \cdot \pi \cdot 251k \cdot 75.3} = 1.4\text{nF}$$

$$C_2 = \frac{1}{18 \cdot \pi \cdot 251k \cdot 75.3} = 0.94\text{nF}$$

R_1 = 75.3Ω

Register Programming

Reg01 = h3A

Reg02 = h00

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From Table 1, FILT = 0 for a 61.44MHz reference frequency. Next, convert 7dBm into V_{P-P}. For a sine wave, use the following equation with R = 50:

$$V_{P-P} \cong \sqrt{R} \bullet 10^{(dBm-21)/20} \quad (21)$$

This gives V_{P-P} = 1.41V, and, according to Table 2, set BST = 1.

Reg03 = h7A

Set the B value:

Reg04 = hA3

Write new R and N values:

Reg05 = h04

Reg06 = h50

Write CP values:

Reg07 = h07

Write P and MUTEx values:

Reg08 = h00

Write M divider values using Table 15:

Reg09 = h9D

Reg0B = h92

Reg0D = h92

Reg0F = h95

OUT4 runs the FPGA management clock which is made continuous by turning off synchronization and not muting during VCO calibration. Use Table 15 for the M4 divider value:

Reg11 = h06

Once all the registers defined above have been written and $\overline{CS}$ is driven back high, the part will initiate a CAL routine and the loop will lock. This can be monitored by reading Reg00 and waiting until LOCK = 1 or by observing the STAT pin going to a logic low.

Delay Settings and Synchronization

The outputs in this example are now running at the desired frequency, but have random phase relationships with each other. The delay settings in this example need to be adjusted to make sure the SYSREF rising edge occurs before the coincident rising edges of the ADC clock and FPGA clock. The propagation delay of the 1:3 fanout buffer on SYSREF needs to be compensated in the calculations. It is important to know the setup times of SYSREF to the ADC clock and SYSREF to the FPGA clock as well as the maximum propagation delay of the fanout buffer. In this example, the setup time for the ADC is 200ps and the FPGA is 250ps. The following equation calculates the setup time, t_{SETUP}:

t_{SETUP} = MAX(200ps, 250ps) = 250ps

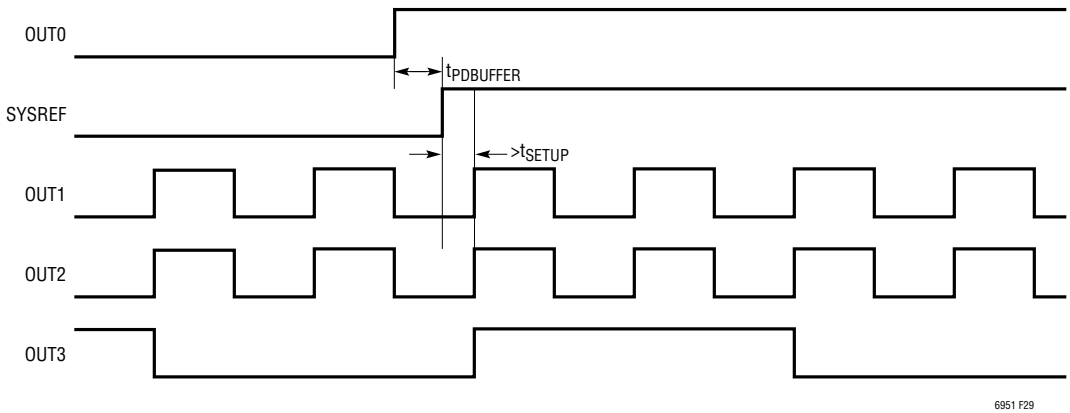

Figure 29. Outputs after SSYNC at SYSREF Rising for the JESD204B Subclass 1 Example

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The fanout buffer propagation delay, $t_{PDBUFFER}$, is 500ps. The minimum amount of setup time from OUT0 is:

$$t_{DOUT0} = t_{SETUP} + t_{PDBUFFER} = 750ps$$

The delay time in the LTC6951 for Dx = 1 is:

$$t_{1Dx} = \frac{P}{f_{VCO}} = 406.9ps$$

To meet setup timing the following equation must be solved for Dx:

$$t_{1Dx} \bullet Dx > t_{DOUT0}$$

$$Dx > \frac{t_{DOUT0}}{t_{1Dx}} > \frac{750ps}{406.9ps} > 1.84$$

Since Dx is an integer, it must be rounded up. Therefore OUT0 must occur at least 2 delay settings, or cycles, before OUT1, OUT2 and OUT3. Board and routing delays need to be considered as well and may cause modifications to these calculations. Since all delay settings are positive numbers, OUT0 will be set to have 0 delay and the other outputs delayed by 2 cycles to achieve the desired result. The new delay settings to program are D0 = 0 and D1 = D2 = D3 = 2:

Reg0A = h00

Reg0C = h02

Reg0E = h02

Reg10 = h02

There is no need to program Reg12 since OUT4 has synchronization disabled. In order for the delay settings to take effect, the part needs to be synchronized and the simplest way to accomplish this is to write the SSYNC bit to a 1 (Note: Hold the SYNC pin at a logic low):

Reg02 = h04

After waiting a minimum of 1ms, write Reg02 again:

Reg02 = h00

Once the internal synchronization process completes, the outputs will be aligned as shown in Figure 29 at the rising edge of SYSREF.

JESD204B SYSREF Considerations

The full procedure for JESD204B subclass 1 alignment is beyond the scope of this data sheet, but the SYSREF pulses may be turned off once lane alignment is achieved to save power and reduce possible beat frequencies in the system. To keep SYSREF synchronized to the ADC and FPGA clocks, it is important to keep the SYSREF divider M0 running at all times. As long as the 1:3 fanout buffer has an enable pin as shown in Figure 28, power down the OUT0 buffer when SYSREF is not needed and disable the fanout buffer. Using Table 16, set MC0[1:0] = 2 and write the register:

Reg09 = AD

When SYSREF is needed again write the register:

Reg09 = 9D

REFERENCE SOURCE CONSIDERATIONS

A high quality signal must be applied to the $REF^{\pm}$ inputs as they provide the frequency reference to the entire PLL. As mentioned previously, to achieve the part's in-band phase noise performance, apply a sine wave of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 40V/µs.

The LTC6951 may be driven single-ended to CMOS levels (greater than $2.7V_{P-P}$). Apply the reference signal at REF^{+}, and bypass REF^{-} to GND with a 47pF capacitor. The BST bit must also be set to "0", according to guidelines given in Table 2. Setting FILT to "0" is recommended since the input is a square wave.

The LTC6951 achieves an in-band normalized phase noise floor L_{NORM} = –229dBc/Hz typical. To calculate its equivalent input phase noise floor L_{IN}, use Equation 22.

$$L_{IN} = L_{NORM} + 10 \bullet \log_{10}(f_{REF}) \quad (22)$$

For example, using a 10MHz reference frequency gives an input phase noise floor of –159dBc/Hz. The reference frequency source's phase noise must be at least 3dB better than this to prevent limiting the overall system performance.

APPLICATIONS INFORMATION

IN-BAND OUTPUT PHASE NOISE

The in-band phase noise floor L_{OUT} produced at f_{OUTx} may be calculated by using Equation 23.

$$L_{OUT} = L_{NORM} + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}\left(\frac{f_{OUTx}}{f_{PFD}}\right) \quad (23)$$

or

$$L_{OUT} = L_{NORM} + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}\left(\frac{N}{P \bullet Mx}\right)$$

where L_{NORM} is –229dBc/Hz.

As can be seen, for a given PFD frequency f_{PFD}, the output in-band phase noise increases at a 20 dB-per-decade rate with the N divider count. So, for a given output frequency f_{OUTx}, f_{PFD} should be as large as possible (or N should be as small as possible) while still satisfying the application's frequency step size requirements.

OUTPUT PHASE NOISE DUE TO 1/F NOISE

In-band phase noise at very low offset frequencies may be influenced by the LTC6951's 1/f noise, depending upon f_{PFD}. Use the normalized in-band 1/f noise $L_{1/f}$ of –277dBc/Hz with Equation 24 to approximate the output 1/f phase noise at a given frequency offset f_{OFFSET}:

$$L_{OUT(1/f)}(f_{OFFSET}) = L_{1/f} + 20 \bullet \log_{10}(f_{OUTx}) - 10 \bullet \log_{10}(f_{OFFSET}) \quad (24)$$

Unlike the in-band noise floor L_{OUT}, the 1/f noise $L_{OUT(1/f)}$ does not change with f_{PFD}, and is not constant over offset frequency. See Figure 30 for an example of in-band phase noise for f_{PFD} equal to 5MHz and 100MHz. The total phase noise will be the summation of L_{OUT} and $L_{OUT(1/f)}$.

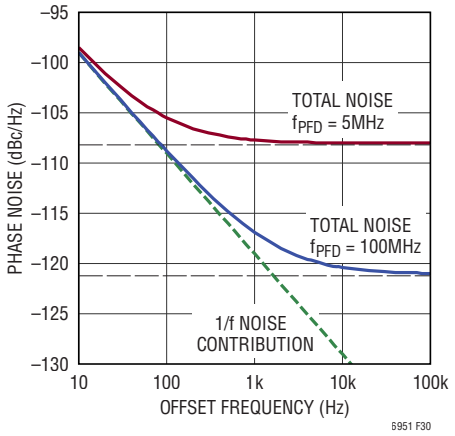


Figure 30. Theoretical In-Band Noise, f_{OUTx} = 2500MHz

REFERENCE SIGNAL ROUTING, SPURIOUS, AND PHASE NOISE

The charge pump operates at the PFD's comparison frequency f_{PFD}. The resultant output spurious energy is small and is further reduced by the loop filter before it modulates the VCO frequency.

However, improper PCB layout can degrade the LTC6951's inherent spurious performance. Care must be taken to prevent the reference signal f_{REF} from coupling onto the VCO's tune line, or into other loop filter signals. Example suggestions are the following.

1) Do not share power supply decoupling capacitors between same-voltage power supply pins.
2) Use separate ground vias for each power supply decoupling capacitor, especially those connected to V_{REF}^+, V_D^+, V_{OUT}^+, V_{RF}^+, V_{CP}^+, and V_{VCO}^+.
3) Physically separate the reference frequency signal from the loop filter and VCO.
4) *Do not place a trace between the CM_A, CM_B, and CM_C pads underneath the package, as worse phase noise could result.*

APPLICATIONS INFORMATION

REFERENCE SIGNAL AND SYNC TIMING FOR SR AND SN MODES

When RAO is set to a "1", bits SN and SR set to a "1" allow precise timing between the REF± inputs and the SYNC input. The LTC6951 is designed to allow sine wave or square wave reference inputs at various levels and all settings of BST or FILT and have consistent performance with respect to setup and hold times of the SYNC pulse. The parameters t_{SS} and t_{SH} are tested and specified for CMOS levels applied to REF+ and SYNC having the performance characteristics shown in Figure 31 for SR and Figure 32 for SN.

The reference is still required to be a high quality signal and is best routed on 50Ω transmission lines. Because CMOS drivers typically are not capable of driving 50Ω, it is recommended to put 100Ω in series with the reference output before being applied to the transmission line, and loaded with 50Ω to GND as close to the LTC6951 as possible. See Reference Source Considerations above. The rise and fall times of the SYNC and REF+ signals are 1ns at the tester.

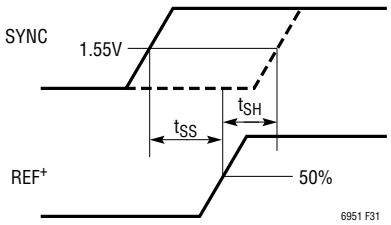


Figure 31. Rising SYNC to REF Timing Detail (RAO = SR = 1)

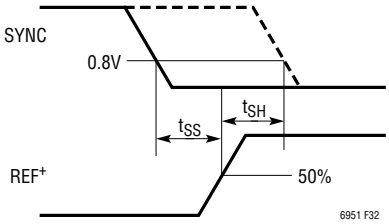


Figure 32. Falling SYNC to REF Timing Detail (RAO = SN = 1)

SUPPLY BYPASSING AND PCB LAYOUT GUIDELINES

Care must be taken when creating a PCB layout to minimize power supply decoupling and ground inductances.

All power supply V+ pins should be bypassed directly to the ground plane using either a 0.01µF or a 0.1µF ceramic capacitor as called out in the Pin Functions section as close to the pin as possible. Multiple vias to the ground plane should be used for all ground connections, including to the power supply decoupling capacitors.

The package's exposed pad is a ground connection, and must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance (see Figure 33 for an example). An example of grounding for electrical and thermal performance can be found on the DC2248A layout. See *QFN Package Users Guide*, page 8, on Linear Technology website's Packaging Information page for specific recommendations concerning land patterns and land via solder masks. A link is provided below.

http://www.linear.com/docs/14077

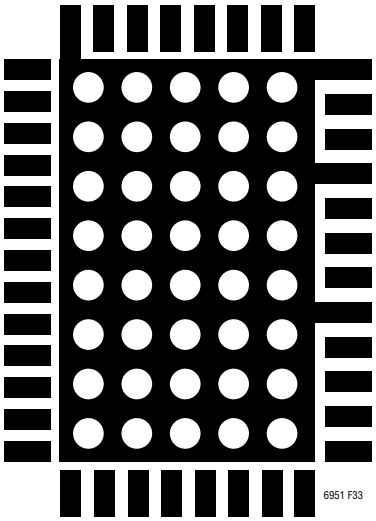


Figure 33. PCB Top Metal Layer Pin and Exposed Ground Pad Design. Pins 25, 29, 32, and 40 Are Signal Ground and Connected Directly to the Exposed Pad Metal

ADC CLOCKING AND JITTER REQUIREMENTS

Adding noise directly to a clean signal clearly reduces its signal to noise ratio (SNR). In data acquisition applications, digitizing a clean signal with a noisy clock signal also degrades the SNR. This issue is best explained in

APPLICATIONS INFORMATION

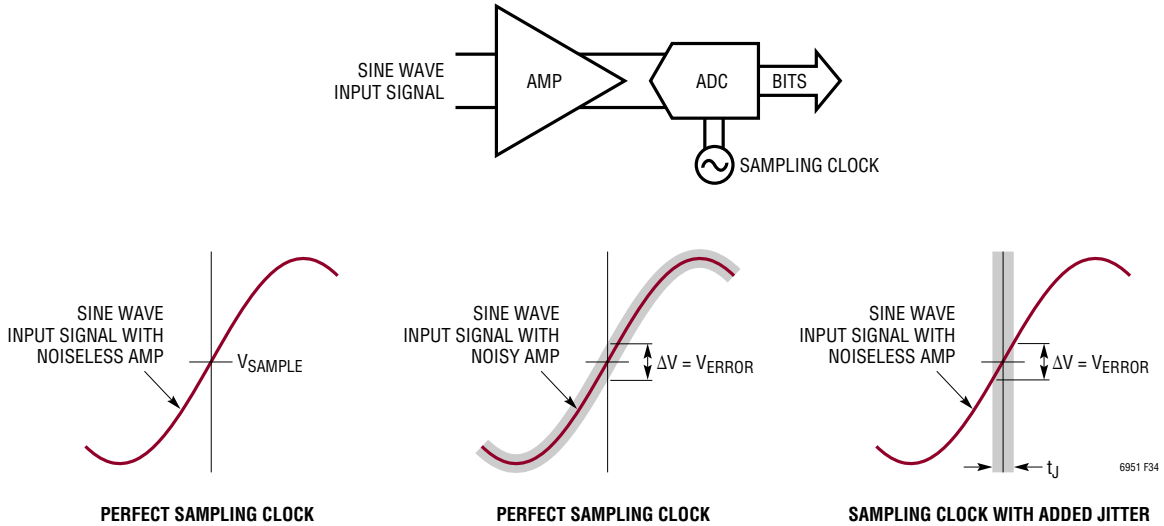


Figure 34. A Typical Data Acquisition Circuit Showing the Sampling Error Effects of a Noisy Amplifier and a Jittery Sampling Clock

the time domain using jitter instead of phase noise. For this discussion, assume that the jitter is white (flat with frequency) and of Gaussian distribution.

Figure 34 shows a sine wave signal entering a typical data acquisition circuit composed of an ADC, an input signal amplifier and a sampling clock. Also shown are three signal sampling scenarios for sampling the sine wave at its zero crossing.

In the first scenario, a perfect sine wave input is buffered by a noiseless amplifier to drive the ADC. Sampling is performed by a perfect, zero jitter clock. Without any added noise or sampling clock jitter, the ADC's digitized output value is very clearly determined and perfectly repeatable from cycle to cycle.

In the second scenario, a perfect sine wave input is buffered by a noisy amplifier to drive the ADC. Sampling is performed by a perfect, zero jitter clock. The added noise results in an uncertainty in the digitized value, causing an error term which degrades the SNR. The degraded SNR in this scenario, from adding noise to the signal, is expected.

In the third scenario, a perfect sine wave input is buffered by a noiseless amplifier to drive the ADC. Sampling is performed by a clock signal with added jitter. Note that as the signal is slewing, the jitter of the clock signal leads to an uncertainty in the digitized value and an error term just as in the previous scenario. Again, this error term degrades the SNR.

A real-world system will have both additive amplifier noise and sample clock jitter. Once the signal is digitized, determining the root cause of any SNR degradation – amplifier noise or sampling clock jitter – is essentially impossible.

Degradation of the SNR due to sample clock jitter only occurs if the analog input signal is slewing. If the analog input signal is stationary (DC) then it does not matter when in time the sampling occurs. Additionally, a faster slewing signal yields a greater error (more noise) than a slower slewing signal. Figure 35 demonstrates this effect. Note how much larger the error term is with the fast slewing signal than with the slow slewing signal. To maintain the data converter's SNR performance, digitization of high input frequency signals requires a clock with much less jitter than applications with lower frequency input signals.

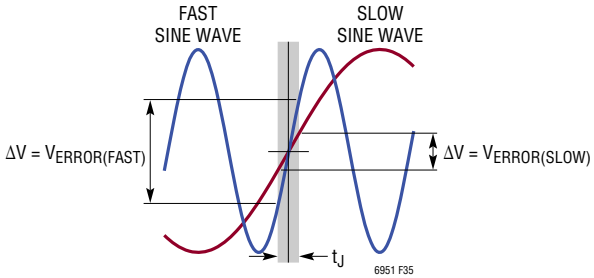


Figure 35. Fast and Slow Sine Wave Signals Sampled with a Jittery Clock

APPLICATIONS INFORMATION

It is important to note that *the frequency of the analog input signal determines the sample clock's jitter requirement. The actual sample clock frequency does not matter.* Many ADC applications that undersample high frequency signals have especially challenging sample clock jitter requirements.

The previous discussion was useful for gaining an intuitive feel for the SNR degradation due to sampling clock jitter. Quantitatively, the actual sample clock jitter requirement for a given application is calculated as follows:

$$t_{J(TOTAL)} = \frac{10^{\frac{-SNR_{dB}}{20}}}{2 \bullet \pi \bullet f_{SIG}} \quad (25)$$

where f_{SIG} is the highest frequency signal to be digitized expressed in Hz, SNR_{dB} is the SNR requirement in decibels and $t_{J(TOTAL)}$ is the total RMS jitter in seconds. The total jitter is the RMS sum of the ADC's aperture jitter and the sample clock jitter calculated as follows:

$$t_{J(TOTAL)} = \sqrt{t_{J(CLK)}^2 + t_{J(ADC)}^2} \quad (26)$$

Alternatively, for a given total jitter, the attainable SNR is calculated as follows:

$$SNR_{dB} = -20\log_{10}\left(2 \bullet \pi \bullet f_{SIG} \bullet t_{J(TOTAL)}\right) \quad (27)$$

These calculations assume a full-scale sine wave input signal. If the input signal is a complex, modulated signal with a moderate crest factor, the peak slew rate of the signal may be lower and the sample clock jitter requirement may be relaxed.

These calculations are also theoretical. They assume a noiseless ADC with infinite resolution. All realistic ADCs have both added noise and a resolution limit. The limitations of the ADC must be accounted for to prevent over specifying the sampling clock.

Figure 36 plots the previous equations and provides a simple, quick way to estimate the sampling clock jitter requirement for a given input signal or the expected SNR performance for a given sample clock jitter.

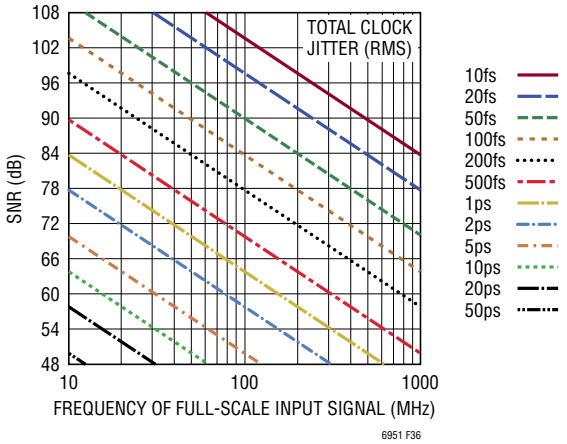


Figure 36. SNR vs Input Signal Frequency vs Sample Clock Jitter

MEASURING CLOCK JITTER INDIRECTLY USING ADC SNR

For some applications, integrating a clock generator's phase noise within a defined offset frequency range (i.e. 12kHz to 20MHz) is sufficient to calculate the clock's impact on the overall system performance. In these situations, the RMS jitter can be calculated from a phase noise measurement.

However, other applications require knowledge of the clock's phase noise at frequency offsets that exceed the capabilities of today's phase noise analyzers. This limitation makes it impossible to calculate jitter from a phase noise measurement.

The RMS jitter of an ADC clock source can be indirectly measured by comparing a jitter dominated SNR measurement to a non-jitter dominated SNR measurement. A jitter dominated SNR measurement (SNR_{JITTER}) is created by applying a low jitter, high frequency full-scale sine wave to the ADC analog input. A non-jitter dominated SNR measurement (SNR_{BASE}) is created by applying a very low amplitude (or low frequency) sine wave to the ADC analog input. The total clock jitter ($t_{J(TOTAL)}$) can be calculated using Equation 28.

APPLICATIONS INFORMATION

$$T_{J(TOTAL)} = \frac{10^{\frac{1}{2}\log_{10}\left[10^{-\left(\frac{SNR_{JITTER}}{10}\right)} - 10^{-\left(\frac{SNR_{BASE}}{10}\right)}\right]}}{2\pi f_{IN}} \quad (28)$$

Assuming the inherent aperture jitter of the ADC ($t_{J(ADC)}$) is known, the jitter of the clock generator ($t_{J(CLK)}$) is obtained using Equation 26.

ADC SAMPLE CLOCK INPUT DRIVE REQUIREMENTS

Modern high speed, high resolution ADCs are incredibly sensitive components able to match laboratory instruments in many regards. With wide bandwidth and wide dynamic range, noise or interfering signals on the analog signal input, the voltage reference or the sampling clock input can easily appear in the digitized data. To deliver the full performance of any ADC, the sampling clock input must be driven with a clean, low jitter signal.

Figure 37 shows a simplified version of a typical ADC sample clock input. In this case the input pins are labeled ENC± for Encode while some ADCs label the inputs CLK± for Clock. The input is composed of a differential limiting amplifier stage followed by a buffer that directly controls the ADC's track and hold stage.

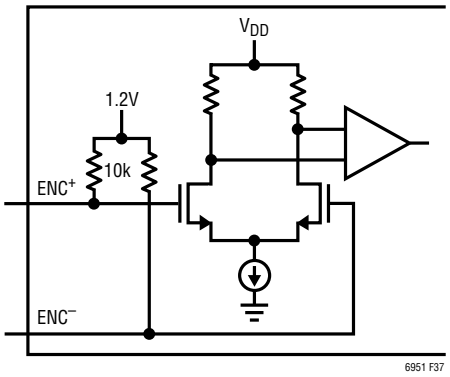


Figure 37. Simplified Sample Clock Input Circuit

The sample clock input amplifier also benefits from a fast slewing input signal as the amplifier has noise of its own. By slewing through the crossover region quickly, the amplifier noise creates less jitter than if the transition were slow.

As shown in Figure 37, the ADC's sample clock input is typically differential with a differential sampling clock delivering the best performance. Figure 37 also shows the sample clock input having a different common mode input voltage than the LTC6951's CML outputs. Most ADC applications will require AC coupling to convert between the two common mode voltages.

The LTC6951's CML outputs (OUT0, OUT1, OUT2, OUT3) are recommended for the best jitter performance to drive sample clock inputs.

TRANSMISSION LINES AND TERMINATION

Interconnection of high speed signaling with fast rise and fall times requires the use of transmission lines with properly matched termination. The transmission lines may be stripline, microstrip or any other design topology. A detailed discussion of transmission line design is beyond the scope of this data sheet. Any mismatch between the transmission line's characteristic impedance and the terminating impedance results in a portion of the signal reflecting back toward the other end of the transmission line. In the extreme case of an open or short circuit termination, all of the signal is reflected back. This signal reflection leads to overshoot and ringing on the waveform. Figure 38 shows the preferred method of far end termination of the transmission line.

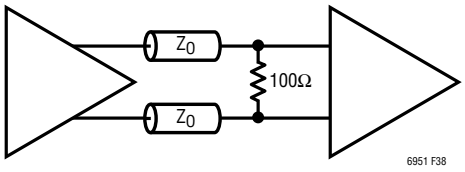


Figure 38. Far End Transmission Line Termination (Z_0 = 50Ω)

Using the LTC6951 to Drive ADC Sample Clock Inputs

As noted earlier, the LTC6951's CML outputs are recommended for the best jitter performance. These outputs are designed to interface with standard CML or LVPECL devices while driving transmission lines with far end termination.

APPLICATIONS INFORMATION

Figure 39 shows DC-coupled and AC-coupled output configurations for the CML outputs OUT0, OUT1, OUT2, and OUT3.

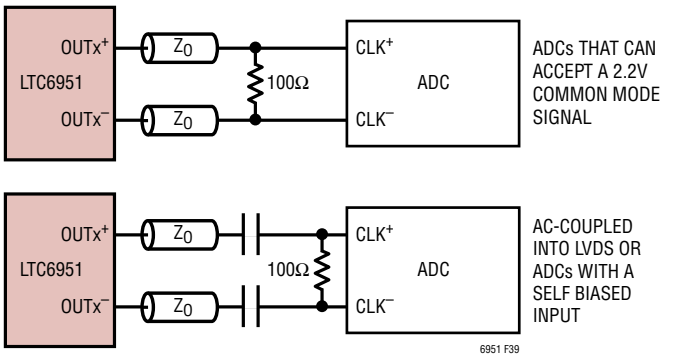


Figure 39. OUTx CML Connections to ADC Sample Clock Inputs (Z_O = 50Ω)

While the CML outputs provide the best ADC sample clock driver performance, the LVDS output can still provide very good performance. Compared to the CML outputs, the LVDS output has a lower frequency limit and a slightly higher phase noise floor.

Figure 40 shows DC-coupled and AC-coupled output configurations for the LVDS output OUT4.

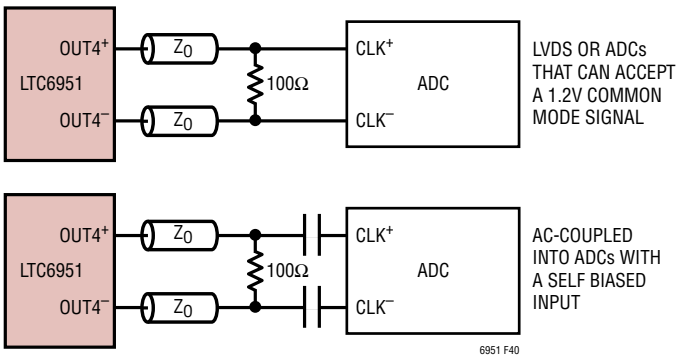


Figure 40. OUT4 LVDS Connections to ADC Sample Clock Inputs (Z_O = 50Ω)

Measuring Differential Spurious Signals Using Single-Ended Test Equipment

Using a spectrum analyzer to measure spurious signals on the single-ended output of a clock generation chip will give pessimistic results, particularly for outputs that approximate square waves. There are two reasons for this.

First, since the spurious energy is often an AC signal superimposed on the power supply, a differential output will reject the spurs to within the matching of the positive and negative outputs. Observing only one side of the differential output will provide no rejection.

Second, and most importantly, the spectrum analyzer will display all of the energy at its input, including amplitude modulation that occurs at the top and bottom pedestal voltage of the square wave. Only amplitude modulation near a zero crossing will affect the clock.

The best way to remove this measurement error is to drive the clock generator output differentially into a limiting buffer on a separate clean power supply. One of the differential outputs of the limiting buffer can then connect to a spectrum analyzer to correctly measure the spurious energy. An example of this technique using the LTC6951 as the clock generator and an LTC6954 as the limiter is shown in Figure 41.

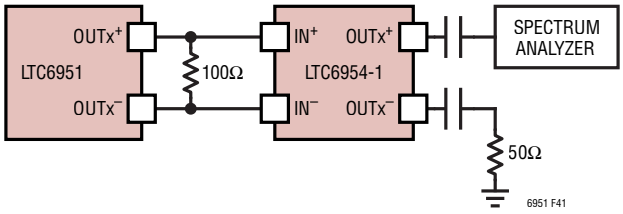
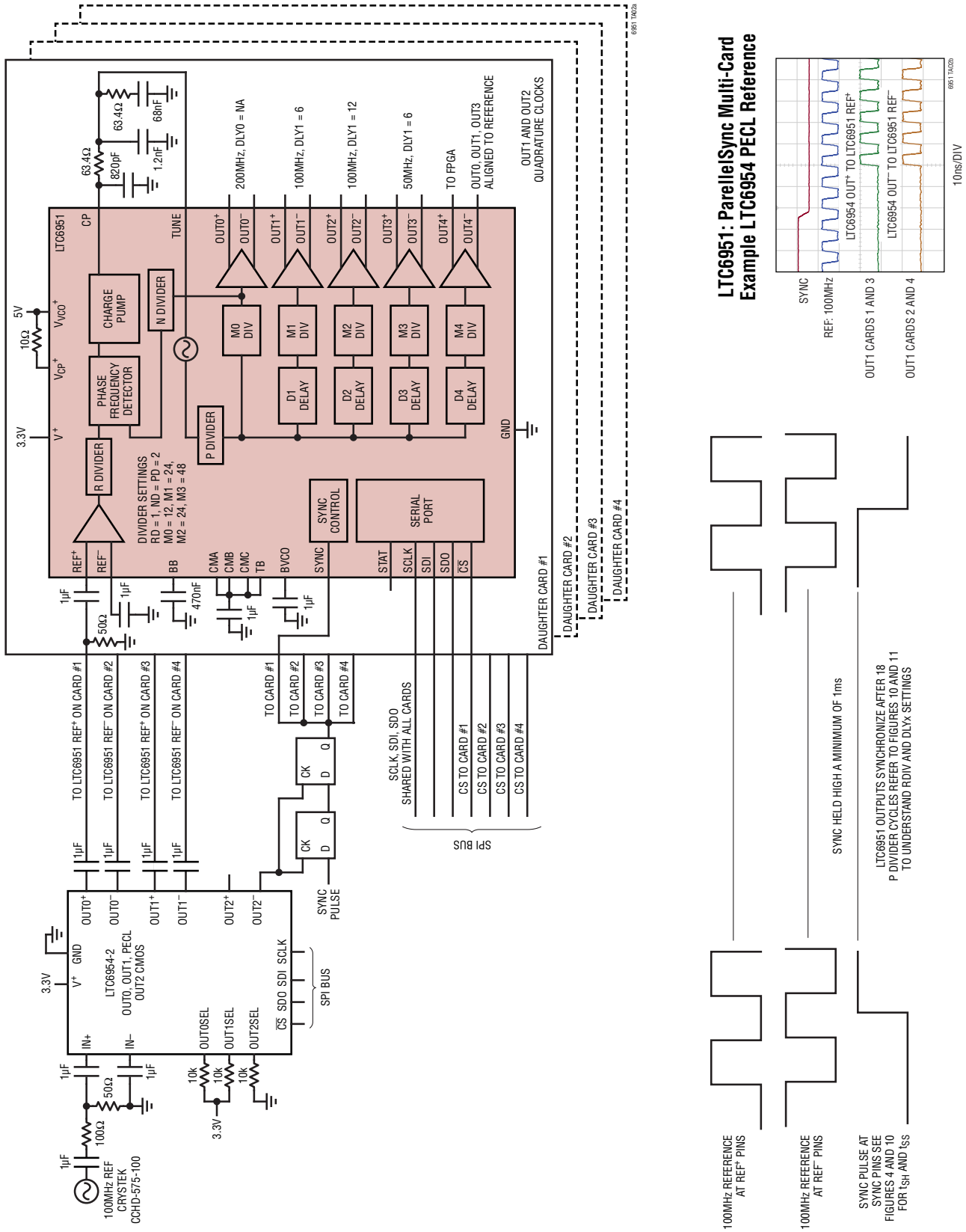
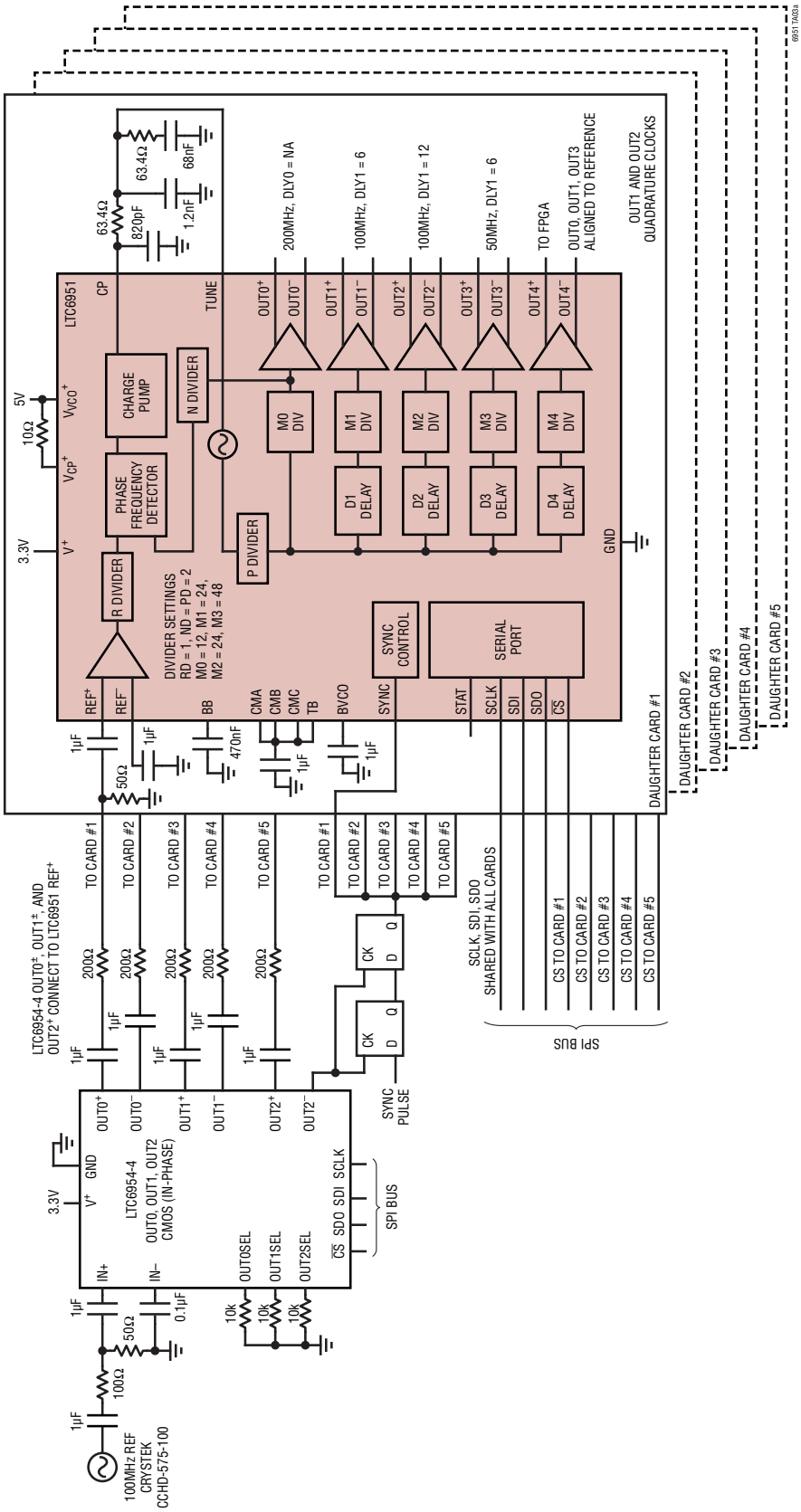


Figure 41. Example of Spurious Measurement Technique

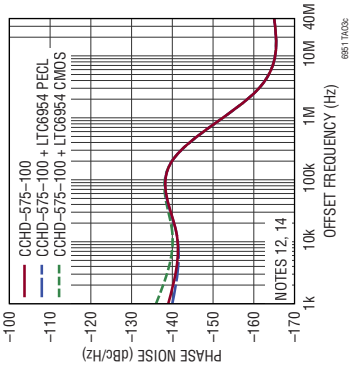
TYPICAL APPLICATIONS



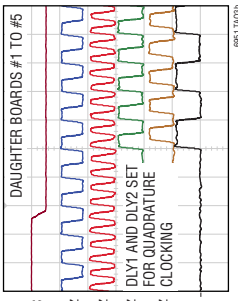
TYPICAL APPLICATIONS



LTC6951 Phase Noise vs Different Reference Inputs, f_{OUT0} = 200MHz



LTC6951: ParallelSync Multi-Card Example LTC6954-4 CMOS Reference



ParallelSync Mode Reference Distribution Selection Table

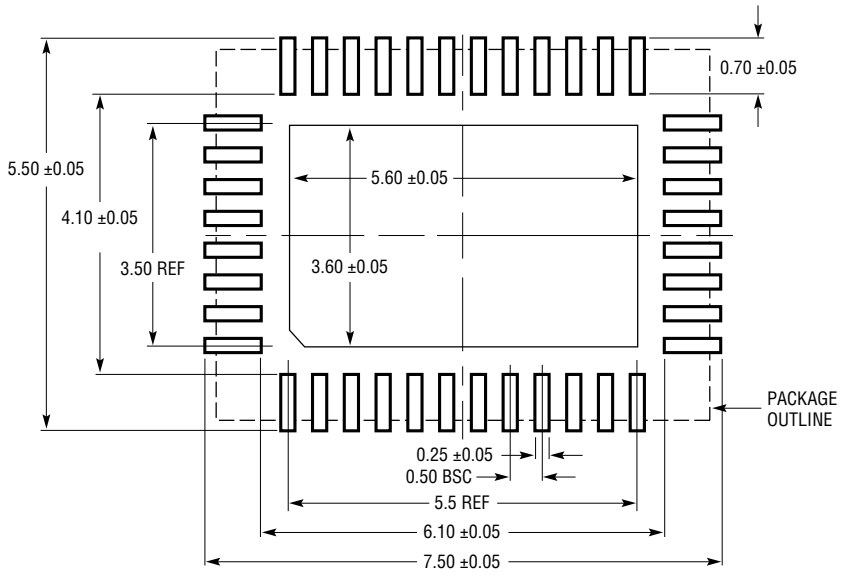
NUMBER OF LTC6951s	LTC6954-2 (PECL)	LTC6954-4 (CMOS)
2	Preferred	Not Recommended
3 or 4	Optimal Close in Phase Noise (See Plot)	Optimal Skew; Avoids Alternating LTC6951 REF± with LTC6954 OUTx±
5	Not Recommended	

Note: To drive more than 5 LTC6951s, the LTC6950 can be used for reference distribution.

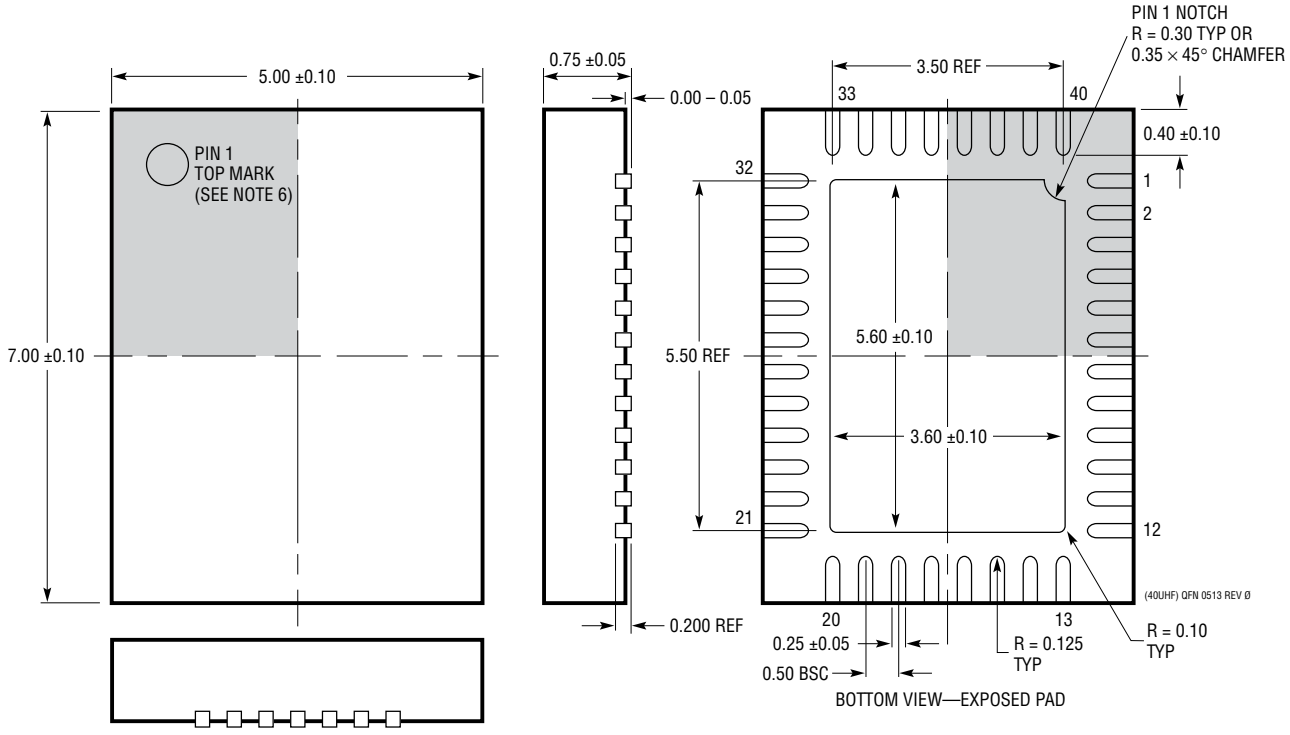
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6951#packaging for the most recent package drawings.

UHF Package
40-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1951 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



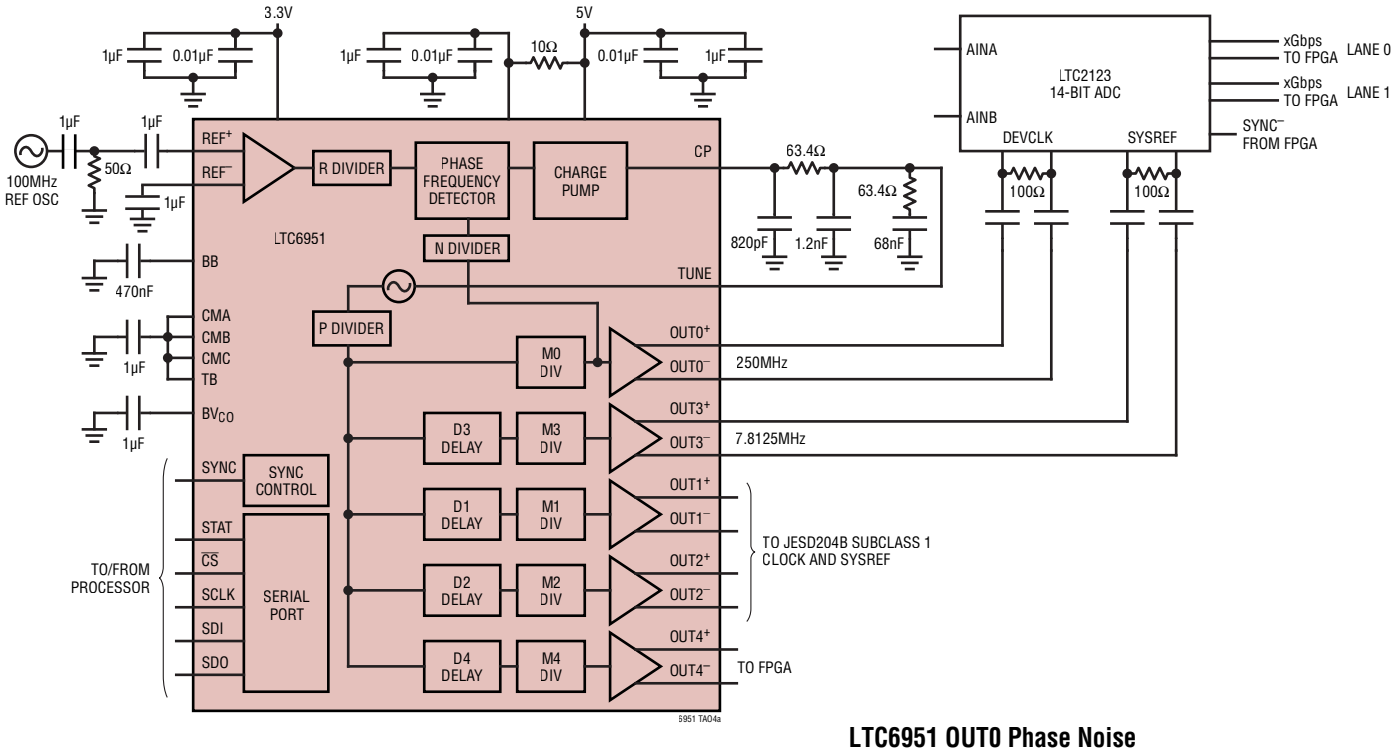
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

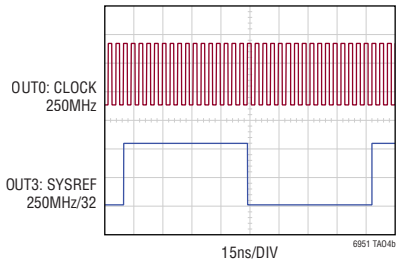
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/17	Units and text edits	4, 13, 23, 24, 27, 44, 45, 49
		Edit to LVPECL schematic in Figure 2	16
		Table 21: ALCEN default value and Mute0 description updated	30
		Charge Pump Function and Current Programming section changed to CP[2:0]	36

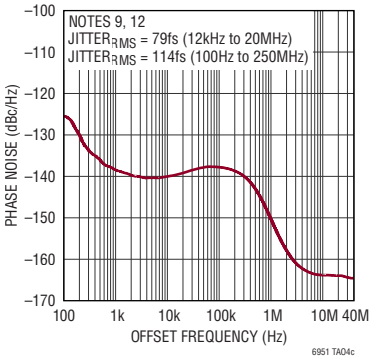
TYPICAL APPLICATION



LTC6951 JESD204B Subclass 1 Clock and SYSREF



LTC6951 OUT0 Phase Noise
f_{OUT0} = 250MHz, P = 2, Mx = 8



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
PLLs and Clock Distribution		
LTC6950	1.4GHz Low Phase Noise, Low Jitter PLL with Clock Distribution	Four Independent LVPECL Outputs with 18fs$_{RMS}$ Additive Jitter (12kHz to 20MHz)
LTC6954	Low Phase Noise, Triple Output Clock Distribution Divider/Driver	LVPECL, LVDS and CMOS Outputs with < 20fs$_{RMS}$ Additive Jitter (12kHz to 20MHz)
ADCs		
LTC2209/LTC2208	16-Bit, 160Msps/135Msps ADCs	77.3dB/77.7dB SNR, 100dB SFDR, 9mm × 9mm QFN Package
LTC2107	16-Bit, 210Msps ADC	80dB SNR, 98dB SFDR, 7mm × 7mm QFN Package
LTC2123/LTC2122	14-Bit, 250Msps/170Msps Dual ADCs with JESD204B Outputs	70dB SNR, 90dB SFDR, Single 1.8V Supply, 7mm × 7mm QFN Package

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